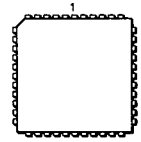
FEATURES

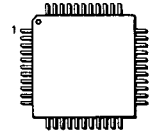
- ☐ Low Power
  - Single supply +5V ± 10%
  - 200mw (typical) operating
  - 60mw (typical) standby excluding SC11198
- ☐ Fax Modes
  - V.29, V.27ter, V.21 Channel 2
- ☐ Voice Mode (SC11087)
  - 10 bit linear
  - 8 bit μ-Law
- ☐ Serial FMAP interface
- ☐ Controller Interface
  - Dual port RAM
- ☐ DTMF detect
- ☐ DTE Interface
  - Parallel PC bus
  - RS232C CCITT V.24 serial
- ☐ Equalizer
  - Automatic adaptive receive equalize
  - Selectable fixed compromise
- ☐ Small Size
  - PLCC or PQFP packages
- ☐ 200 ns Instruction cycle time
- ☐ 256 x 16 RAM
- ☐ Internal ROM program
- ☐ Group 1 and Group 2

44 PIN PLCC PACKAGE



SC11087CV
SC11198CV

44 PIN PQFP (14mm) PACKAGE



SC11087CQ
SC11198CQ

GENERAL DESCRIPTION

The SC11087 series products are low power facsimile modem Digital Signal Processors designed for use with Sierra's SC11086 and SC11196 families of Fax Modem Analog Processors (FMAP).

Together, the two-chip sets comprise a complete modem data pump supporting CCITT facsimile standards up to 9600 bit/s. All models support group 3, V.21 channel 2, V.27 ter and V.29 standards. In addition the SC11198 supports groups 1 & 2 modes. The SC11087 features voice mail modes including simultaneous voice transmission & DTMF tone detection and optional μ-LAW compression. The SC11087 family, when combined with a Sierra data modem and fax AFE, forms a complete 2400 bit/s data/9600 bit/s fax modem data pump supporting synchronous and asynchronous full duplex V.21, V.22, V.22bis, V.23, Bell 103, Bell 212, and 212A.

These sets includes DTMF tone detection, programmable transmit level, ring input and elimination of external op amp for dial up line applications.

The SC11086 and SC11198 chipset can be used with Sierra's SK0611 and other chipsets to build a complete intelligent Fax and Data modem compatible with EIA class 2 capabilities. A special four chip kit, SQ0196, is offered for this application. Firmware and application software are available.

BLOCK DIAGRAM

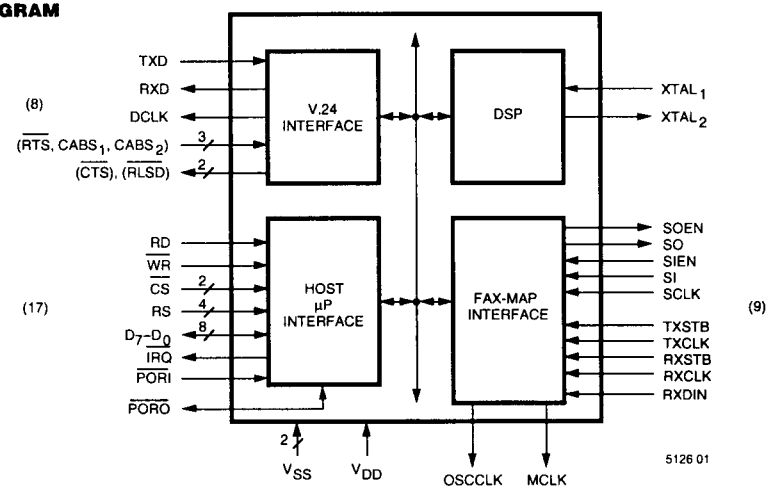


Figure 1.

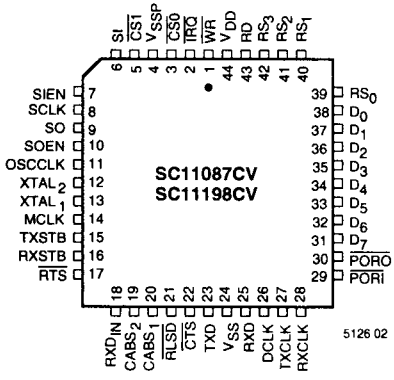
Rev 1.0

PIN DESCRIPTIONS

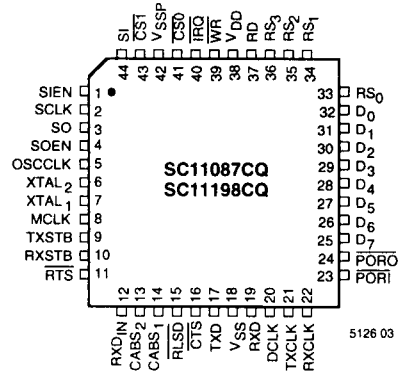
PIN NAME	PIN NUMBER SC11087CV SC11198CV PLCC	PIN NUMBER SC11087CQ SC11198CQ PQFP	DESCRIPTION
$CABS_1$	20	14	**INPUT. TTL WITH PULLUP.** Cable Select 1
$CABS_2$	19	13	**INPUT. TTL WITH PULLUP.** Cable Select 2
$\overline{CS_1}$	5	43	**INPUT. TTL.** Register Bank 1 Chip Select
$\overline{CS_0}$	3	41	**INPUT. TTL.** Register Bank 0 Chip Select
$\overline{CTS}$	22	16	**OUTPUT. OPEN-DRAIN WITH PULLUP.** Clear-to-Send
D_7–D_0	31–38	25–32	**INPUT/OUTPUT. TTL TRANSCEIVER.** 8 Bit Data Bus
DCLK	26	20	**OUTPUT. OPEN-DRAIN WITH PULLUP.** Data Clock
$\overline{IRQ}$	2	40	**OUTPUT. OPEN-DRAIN WITH PULLUP.** Interrupt Request
MCLK	14	8	**OUTPUT. CMOS.** Clock Output (9.792 MHz)
OSCCLK	11	5	**OUTPUT. CMOS.** Oscillator Output (19.6608 MHz)
$\overline{PORI}$	29	23	**INPUT. TTL WITH SCHOTTKY TRIG.** Power-on-Reset Input
$\overline{PORO}$	30	24	**INPUT/OUTPUT. OPEN-DRAIN WITH PULLUP.** Power-on-Reset Input/Output
RD	43	37	**INPUT. TTL.** Read Enable
$\overline{RLSD}$	21	15	**OUTPUT. OPEN-DRAIN WITH PULLUP.** Received Line Signal Detector
RS_0–RS_3	39–42	33–36	**INPUT. TTL.** Register Select Lines
$\overline{RTS}$	17	11	**INPUT. TTL WITH PULLUP.** Request-to-Send
RXCLK	28	22	**INPUT. CMOS.** Receiver Clock
RXD	25	19	**OUTPUT. OPEN-DRAIN WITH PULLUP.** Receiver Data
RXD_{IN}	18	12	**INPUT. CMOS WITH PULLUP.** Receiver Data Input
RXSTB	16	10	**INPUT. CMOS.** Receiver Strobe
SCLK	8	2	**INPUT. CMOS.** Serial Input Clock
SO	9	3	**OUTPUT. CMOS THREE-STATE.** Serial Data Output
SI	6	44	**INPUT. CMOS.** Serial Data Input
SIEN	7	1	**INPUT. CMOS.** Serial Input Enable
SOEN	10	4	**OUTPUT. CMOS.** Serial Output Enable
TXCLK	27	21	**INPUT. CMOS.** Transmitter clock
TXD	23	17	**INPUT. TTL WITH PULLUP.** Transmitter Data
TXSTB	15	9	**INPUT. CMOS.** Transmitter Strobe
V_{DD}	44	38	**POWER.** +5 Volt Supply
V_{SS}	24	18	**POWER.** Ground
V_{SSP}	4	42	**POWER.** Ground
$\overline{WR}$	1	39	**INPUT. TTL.** Write Enable
$XTAL_2$	12	6	**CRYSTAL.** Crystal Output (19.6608 MHz)
$XTAL_1$	13	7	**CRYSTAL.** Crystal Input (19.6608 MHz)

CONNECTION DIAGRAMS

44L PLCC



44L PQFP



FUNCTIONAL DESCRIPTION

The Fax Modem DSP (FMDSP) processor is a DSP engine for Fax Modem applications. It is designed to do all signal processing tasks for a Fax Modem except the sample rate processing for the group 3 receiver, which is done in the FaxMAP front end chip. Since this is a half duplex modem, the maximum computation load is presented by symbol processing for the V.29 receiver, combined with simultaneous tone generation. This includes the following routines which are completed in one V.29 symbol period of 416 µs:

- Equalizer
- Carrier Tracker
- Slicer
- Differential Decoder
- Grey to Binary Converter
- Descrambler
- Sync Recovery PLL
- Tone Generator

Other functions which are handled, but not in the critical path are:

- Group 1 Transmitter and Receiver
- Group 2 Transmitter and Receiver
- V.21 Transmitter and Receiver
- Tone Generators (Including DTMF)
- Tone Detector

Processor Architecture Overview

The FMDSP processor is a 16-bit processor dedicated to the FAX Modem DSP functions. Designed with RISC philosophy, its instructions are mostly single word and execute in a single clock cycle. The processor uses a two stage pipeline, fetch and execute. Therefore, all branch instructions take two clock cycles to execute. Delay Jump Instructions are included to achieve single cycle branch as most RISC processors do.

The FMDSP processor utilizes the so-called Harvard achitecture similar to TMS320. The Data memory space of 512 words total is completely on chip. The program memory is read only. A TMS320-like TBLR instruction is providedto load the coefficient table from the program space into on-chip RAMs.

The FMDSP is organized around one 16 bit data bus and one 9 bit address bus. Except for four hardware registers, all processor resources are addressable Data Memory locations. All I/Os are also memory mapped.

Special hardware is incorporated on-chip to achieve high throughput in critical DSP functions. The most notable is the 16 by 16 hardware multiplier that can do a 2's complement multiplication in 63 ns. An 8 bit accumulator, together with the 16 bit ALU, combine to perform the 24 bit accumulation of multiply results which is 32 bits wide with the lower 7 bits discarded. There is also a 6 bit loop counter used by the RPT and RPT2 instructions to perform loops with zero overhead. Saturation arithmetic is supported by the ALU.

Transmitter Tonal Signaling and Carrier Frequencies

T.30 Tonal Signaling Frequencies

Function	Freq. (Hz) (±0.01%)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group 2 Identification (C12)	1850
Group 2 Command (GC2)	2100
Group 2 Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462
Group 1 White Black	1500 2400

Carrier Frequencies

Function	Freq. (Hz) (±0.01%)
T.3 Carrier (Group 2)	2100
V.27 ter Carrier	1800
V.29 Carrier	1700

Tone Generation

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3400 Hz are attenuated.

Tone Detection

In the 300 bit/s FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory.

V.27ter Short Train

To achieve a successful short train, a long train at the same data rate must precede the short train. In the long train, the host waits until CDET is activated, sets the FRT bit to freeze the equalizer, then reads and stores the taps in the external RAM. In the short train mode, the host waits for the modem to be reconfigured, then starts to write the taps back to the modem. This will allow the modem to train within the shorter period.

Signaling and Data Rates

Specification	Baud Rate (Symbols/Sec.)	Bits per Baud	Data Rate (bit/s) (±0.01%)	Symbol Points
V.29	2400	4	9600	16
V.29	2400	3	7200	8
V.27ter	1600	3	4800	8
V.27ter	1200	2	2400	4
V.21	300	1	300	N/A

Data Encoding

The modem data encoding conforms to CCITT reccommendations V.29 and V.27 ter.

Equalizers

The data pump provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers—Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer is configured as a T/2 equalizer with 32 taps.

Transmitted Data Spectrum

The transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter or V.29 depending on the selected configuration.

Received Signal Frequency Tolerance

The receiver circuit of the modem can adapt to received carrier frequency error of up to ± 10 Hz with less than a 0.2 dB degradation in BER performance. However, the symbol rate must be within 0.01% for proper operation. Group 2 carrier recovery capture range is 2100 ± 30 Hz. The Group 2 receiver operates properly when the carrier is varied by ± 16 Hz at a 0.1 Hz per second rate.

Tone Detection

Three tone detectors are active in the FSK, CPM or TONE mode. In the CPM mode the frequencies default to FR1, FR2, FR3 in memory interface bank 1, register B address (1:B:5-7). The defaults vary depending on the FAX or DATA mode. They may, however, be reprogrammed to specific frequencies by the user. Sierra provides an applcation note to explain how to calculate the coefficients of the filters and program user specific frequencies. Tone detection continues even when tones are transmitted allowing for calling tones to be transmitted during CPM detection.

HDLC Flag Detection

In Group 3 or FSK receive mode, HDLC flag sequence can be detected by enabling the FDEN bit in the interface memory. In Group 3 mode, the hardware 1850/1650 Hz detector is enabled and monitored to determine the presence of flag sequence. In FSK mode, the firmware monitors the received data to decide the flag detection.

Voice Mode Application

When the modem is configured in the voice mode, the 10 bit data are read/written through the interface register 0:1 (MSBs) and 0:0 (LSBs). The data may be sampled at 9600, or 4800 samples per second, depending on the modem chip used.

In the transmit mode, only the 10 MSBs are written to the 10 bit D/A. In the receive mode, the 6 LSBs are filled with zeroes. During voice transmissions, the DTMF receiver is also activated. This allows the host to terminate voice transmission once a DTMF tone is detected.

To use the voice capability, the host processor first sets the DSP to voice mode by writing 82H to register (0:4) and setting SETUP bit (0:E:3) to one. This also enables the DTMF receive function in SC11087. (The SC11198 cannot simultaneously detect DTMF tones while transmitting voice.)

The MDA0 (0:E:0) bit (Modem Data Available) is set by the DSP when it is ready for the host processor to read data fromor write data tothe YSM and/or YSL registers. After the processor has read or written 16 bit data to these RAM locations, it resets MDA0 to "0". In transmit mode the most significant 12 bits of YSM and YSL will be written to the DAC for transmission. In the receive mode, the 10 bit ADC output is written to YSM & YSL and the 4 LSB's are filled with "0's".

Receive Timing

In the receive state, the FDSP provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of the received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ± 1%.

Transmit Level

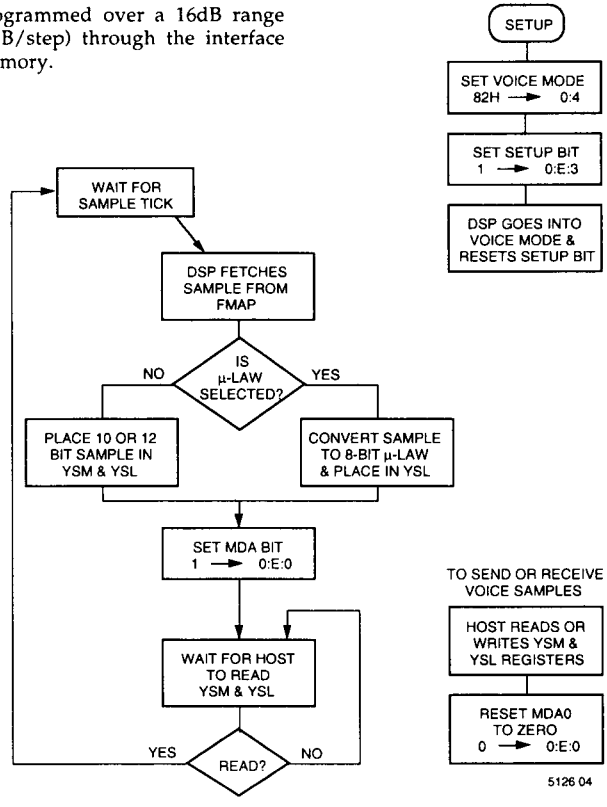
The transmitter output level defaults to -1dBm ±1 dB at power on. When using the default transmit level and driving a 600 ohm load, the TXA output requires a 600 ohm series resistor to provide -1 dBm ±1 dB to the load. The output level can be programmed over a 10 dB range by performing a RAM write operation. The transmit can also be programmed over a 16dB range (1dB/step) through the interface memory.

Transmit Timing

In the transmit state, the FDSP provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz (± 0.01%). In Group 2 and Group 1, DCLK tracks an external 10368 Hz clock. If the external clock input (XCLK) is grounded the Group 1 and Group 2 DCLK is 10372.7 Hz ± 0.01%.
2. *Duty Cycle.* 50 ± 1%

Transmit Data (TXD) must be stable during the 1 microsecond period immediately preceding and the 1 microsecond period immediately following the rising edge of DCLK.



Turn-On Sequence

A total of ten selectable turn-on sequences can be generated by the modem, as defined in Table 1.

Turn-Off Sequence

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy. In V.21 the transmitterturns off within 7 ms after $\overline{RTS}$ goes false. In Group 2 and Group 1 the transmitter turns off within 200 µs after $\overline{RTS}$ goes false.

Clamping

The following clamps are provided with the modem:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector ($\overline{RLSD}$).* $\overline{RLSD}$ is clamped off (squelched) during the time when $\overline{RTS}$ is on.
3. *Extended Squelch.* Optionally, $\overline{RLSD}$ remains clamped off for 130 ms after the turn-off sequence

Response Times of Clear-to-Send ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the length of the training sequence. Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bit/s, and 943 ms for V.27 ter at 2400 bit/s. In V.21 $\overline{CTS}$ turns on in 14 ms or less. In Group 2 $\overline{CTS}$ turns on in 400 µs or less.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

Received Line Signal Detector ($\overline{RLSD}$)

For either V.27 ter or V.29, $\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RLSD}$ off-to-on response time is 15 ± 10 ms. The $\overline{RLSD}$ on-to-off response time for V.27 is 10 ± 5 ms and for V.29 is 30 ± 9 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided:

1. Greater than -43 dBm ($\overline{RLSD}$ on)
   Less than -48 dBm ($\overline{RLSD}$ off)
2. Greater than -47 dBm ($\overline{RLSD}$ on)
   Less than -52 dBm ($\overline{RLSD}$ off)

NOTE
Performance may be at a reduced level when the received signal is less than -43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

Table 1. Turn-On Sequences

Specification	$\overline{RTS}$–$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.29	253 ms	438 ms
V.27 4800 bit/s	708 ms	913 ms
V.27 2400 bit/s	943 ms	1148 ms
V.21 300 bit/s	≤ 14 ms	≤ 14 ms
Group 2	≤ 400 µs	≤ 400 µs

MODES OF OPERATION

The DSP operates in either a serial or a parallel mode.

Serial Mode

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data.

Parallel Mode

The data pump can transfer channel data eight bits at a time via the microprocessor bus.

Mode Selection

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to 1. The modem automatically defaults to the serial mode at power-on. In either mode the modem is configured by the host processor via the microprocessor bus.

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits.

Hardware Circuits

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the Modem Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital or Analog Interface Characteristics.

Microprocessor Interface

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

$CABS_2$	$CABS_1$	Length of 0.4 mm Dia. Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Overhead

Except for the power-on-reset signal $\overline{POR}$, the overhead signals are DC power or ground points. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready for normal use. The POR sequence is reinitiated anytime the + 5V supply drops below + 3.5V for more than 30 ms, or an external device drives pin 29 low for at least 3 µs. When an external low input is applied to pin 29, the modem is ready for normal use approximately 10 ms after the low input is removed. In all cases, the POR sequence requires from 50 ms to 350 ms to complete. The POR sequence leaves the modem configured as follows:

- V.29/9600 bit/s
- T/2 equalizer
- Serial mode
- Training enabled
- Echo protector tone enabled
- No extended squelch
- Higher receive threshold
- Interrupts disabled
- RAM Access S = 00
- RAM Access B = 22
- Eye pattern disabled
- Transmit signal is summed with AUX input before sending to TXA
- Transmit level control with 0dB attenuation
- HDLC flag detection disabled
- Receive input control normal

This configuration is suitable for performing high speed data transfer on the PSTN with the serial data port selected as the input and output point for data terminal equipment (DTE).

Software Signals

The FDSP contains 32 registers to which an external (host) microprocessor has access. Although these registers are within the DSP, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers update at the modem sample rate (9600 bit/s) in the transmit mode and at the selected baud rate in the receive mode. In Group 2 FSK configuration they update at the sample rate of 10368/9600 Hz.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip includes two blocks of 16 registers. The block is specified by Y (0 or 1), the register by Z (0-F), and the bit by Q (0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Status/Control Bits

Modem operation is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined on the Interface Memory table. Bits designated by a '—' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-write-modify operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits are written back into the register of the interface memory.

RAM Data Access

The user can access much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register 0:F (RAM ACCESS S) or 1:F (RAM ACCESS B). The RAM Access Codes table lists access codes for storage in registers 0:F or 1:F and the corresponding diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long.

These bits are written into interface memory registers 0:3, 0:2, 0:1 and 0:0, or 1:3, 1:2, 1:1 and 1:0, in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit 0:5:5 (RAMWS) or bit 1:D:0 (RAMWB) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM in bank 0 or in bank 1, respectively. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bit written in XRAM or YRAM come from registers 1 and 0, with register 1 being the most significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAM Access B bits of register 1:F for chip 1, or by means of 0:5:4 (RAE) and 0:F (RAM Access S) for chip 0. When bit 1:F:7 or 0:5:4 is set to one, the XRAM is selected. When 1:F:7 or 0:5:4 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the modem data available bit 0:E:0 or 1:E:0 (MDA1) is reset to zero. When the FDSP reads or writes register 0, MDA1 is set to a one. When set to a one by the host, bit 0:E:2 or 1:E:2 (IE1) enables the MDA1 bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit 0:E:7 or 1:E:7 (IA1) goes to a one.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem. This information is scaled as shown in the Diagnostic Data Scaling table.

RAM Access Codes

NODE	FUNCTION	ACCESS	RAE	BLOCK	READ REG. NO.
1	Received Signal Samples	40	X	0	2, 3
2	Demodulator Output				NAV
3	Low Pass Filter Output	54	X	0	0, 1, 2, 3
4	Average Power	5C	X	0	2, 3
5	AGC Gain	3C	X	0	2, 3
6	Tone 1 Frequency	71	1	0	0, 1
7	Tone 1 Level	72	1	0	0, 1
8	Tone 2 Frequency	71	0	0	0, 1
9	Tone 2 Level	72	0	0	0, 1
10	Output Level	4C	0	0	0, 1
11	Equalizer Input	40	N.A.	1	0, 1, 2, 3
12	Equalizer Tap Coefficients	01-20	N.A.	1	0, 1, 2, 3
13	Unrotated Equalizer Output	61	N.A.	1	0, 1, 2, 3
14	Rotated Equalizer Output (Received Point—Eye Pattern)	22	N.A.	1	0, 1, 2, 3
15	Decision Points (Ideal)	62	N.A.	1	0, 1, 2, 3
16	Error Vector	63	N.A.	1	0, 1, 2, 3
17	Rotation Angle	00	N.A.	1	0, 1
18	Frequency Correction	A8	N.A.	1	2, 3
19	Eye Quality Monitor (EQM)	AB	N.A.	1	2, 3

RAE = X is don't care since this location should only be read from, and not written to, by the host. N.A. is not applicable since RAE is not used in bank one.

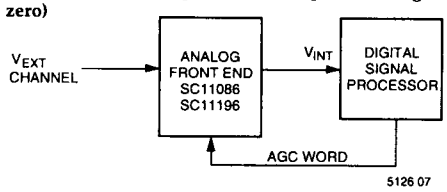
NAV = Not Available

In Group 2 receive mode the modem does the training internally. It does not require the extensive interaction from the external processor.

DIAGNOSTIC DATA SCALING

NODE 1

Received Signal Samples = A/D Sample Word (signed 16 bits, twos complement, unused LSB are filled with zero)



$$V_{IN} = \frac{(\text{A/D Sample Word})_{16}}{40_{16}} \times \frac{3}{256} \text{ Volts}$$

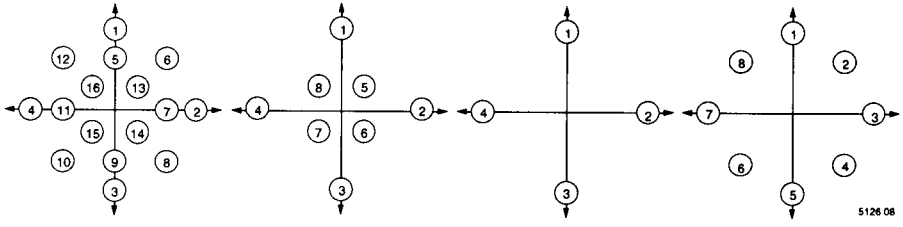
$$V_{EXT} = V_{INT} \; / \; \text{LOG}_{10}^{-1} \frac{\text{AGC Gain (dB)}}{20}$$

5126 eq 1

NODE 3, 11, 13, 14, 15

All Baseband Signal Nodes (32 bits, complex, twos complement)

POINT	CONFIGURATION			
	V.29/9600 X, Y	V.29/7200 X, Y	V.29/4800 & V.27/2400 X, Y	V.27/4800 X, Y
1	0000, 2800	0000, 2400	0000, 1F00	0000, 1F00
2	2800, 0000	2400, 0000	1F00, 0000	1600, 1600
3	0000, D800	0000, DC00	0000, E100	1500, 0000
4	D800, 0000	DC00, 0000	E100,0000	1600, EA00
5	0000, 1800	0C00, 0C00		0000, E100
6	1800, 1800	0C00, F400		EA00, EA00
7	1800, 0000	F400, F400		E100, 0000
8	1800, E800	F400, 0C00		EA00, 1600
9	0000, E800			
10	E800, E800			
11	E800, 0000			
12	E800, 1800			
13	0800, 0800			
14	0800, F800			
15	F800, F800			
16	F800, 0800			



NODE 4

Average Power (16 bits, unsigned)

Typical value: 0889_{16} (corresponding to 0 dBm)

$$\text{Post-AGC Average Power in dBm} = 10 \; \text{Log} \frac{(\text{Average Power Word})_{16}}{889_{16}}$$

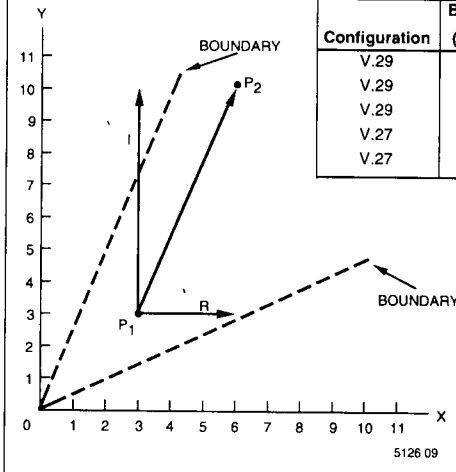
Pre-AGC Power in dBm = Post-AGC Avg. Power in dBm – AGC gain in dB

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
5	**AGC Gain (16 bits, unsigned)** Range: $0FC0_{16}$ to $7FFF_{16}$ for LRTH = 0 (–43 dBm Threshold) 0640_{16} to $7FFF_{16}$ for LRTH = 1 (–47 dBm Threshold) AGC Gain in dB = $50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0.09$
6, 8	**Tone 1 and 2 Frequency (16 bits, unsigned)** N = 6.8267 (Frequency in Hz) Convert N to hexadecimal then store in RAM.
7, 9	**Tone 1 and Tone 2 Level** Calculate the power of each tone independently by using the equation for Output Number given at node 10 with M=16337. Convert these numbers to hexadecimal then store in RAM. Total power transmitted in tone configuration is the result of both tone 1 power and tone 2 power.
10	**Output Level (16 bits, unsigned)** Output Number = M $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store in RAM. M varies depending on configuration. The output level can only be changed after RTS is active. **Configuration** / **M** V.29/9600 — 17408 V.29/7200 — 26880 V.27/4800 — 16640 V.27/2400 — 16640 FSK, Group 1 — 16337 Group 2 — 30976
12	**Equalizer Taps (32 bits, complex, twos complement)** Node 12 is not a single point but is acutally a set of RAM locations containing adaptive equalizer tap coefficients. In V.29 configuration, access codes 01 through 20 hexadecimal represent 32 complex center taps. In V.27 configuration, access codes 01 through 20 hexadecimal represent all 32 complex taps, since the equalizer for V.27 is not as long as the equalizer for V.29. The equalizer tap access codes can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. This sequence is also used in the V.27 short train. The equalizer has 48 taps in V.29 mode and is T/2 spaced only. The 32 center taps can be read out for diagnostic purposes. In V.27 mode the equalizer has 32 taps and all taps can be read out.

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
16	**Error vector (32 bits, complex, twos complement)** Represents the difference between the received point (P2) and the nearest ideal point (P1).

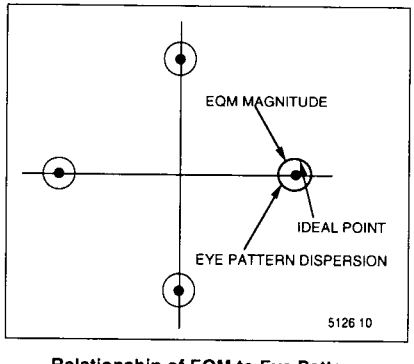


Configuration	Bit Rate (BIT/S)	Registers 3 and 2 Real Error	Registers 1 and 0 Imag. Error	Magnitude $\sqrt{Re^2 + Im^2}$
V.29	9600	$<0C00_{16}$	$<0C00_{16}$	$<0E66_{16}$
V.29	7200	$<2400_{16}$	$<2400_{16}$	$<1AD4_{16}$
V.29	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	2400	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$

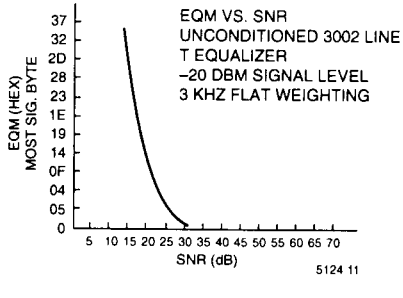
Error Vector Maximum Values

$P_1 = x_1 + iy_1$
$P_2 = x_2 + iy_2$
$P_2 - P_1 = (x_2 - x_1) + i(y_2 - y_1)$
= REAL ERROR + IMAGINARY ERROR

17	**Rotation Angle (16 bits, twos complement)** Represents instantaneous correction for phase and frequency errors Rotation Angle in degrees = $\frac{(\text{Rot. Angle Word})_{16}}{10000_{16}} \times 180$
18	**Frequency Correction (16 bits, twos complement)** Represents componemt of rotation angle caused by frequency error. Range: $FC00_{16}$ to 0400_{16} representing ± 37.5 Hz Frequency Correction in Hz = $\frac{(\text{Freq. Correction Word})_{16}}{10000_{16}} \times$ Baud Rate in Hz
19	**Eye Quality Monitor, EQM (16 bits, unsigned)** Equals the filtered squared magnitude of the error vector. Proportionally to bit error rate is determined by particular application. Stabilizes in approximately 700 baud times from RLSD going active.



Relationship of EQM to Eye Pattern



Typical Eye-Quality Versus Signal-to-Noise Ratio for V.29/9600

Dual Port RAM Memory Interface Definition
Bank 0

Bit / Register	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS						
E	IA0	—	—	SHTR§	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	RAMWS	RAE	EPT	SQEXT	—	LRTH
4	CONFIGURATION							
3	RAM DATA; XSM FREQ MSB							
2	RAM DATA; XSL FREQ LSB							
1	RAM DATA; YSM							
0	RAM DATA; YSL							

Bank 1

Bit / Register	7	6	5	4	3	2	1	0
F	RAM ACCESS							
E	IA1	EYE/TX	=†	TX1	TX0	IE1	AUDIO	MDA1
D	—	—	=	—	—	—	FRT	RAMWB
C	RX0	SETUP2	FDEN	TL3	TL2	TL1	TL0	—
B	FR3	FR2	FR1	—	—	—	—	—
A	—	COL3	COL2	COL1	ROW4	ROW3	ROW2	ROW1
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{\text{PNDET}}$	FLAG	RINGIN	—	—	=	$\overline{\text{CDET}}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{\text{FED}}$	—	—	—	—	=	PD*
4	MUEN§	RDREN§	—	—	=	$\overline{\text{P2DET}}$	CTSP	=
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YSL							

† = Modem internal use position
— Unused position
§ 11087 only

DUAL PORT RAM MEMORY INTERFACE (BANK 0)

Register F Address (0:F:0–7)

Bit Number	Bit Name	Description
0–6		RAM Access. These 7 bits contain the RAM access code used in the read/write RAM location in bank 0.
7	PDM	Parallel Data. PDM = 1 configures the modem in the parallel mode operation which inhibits the diagnostic reading of bank 0.

Register E Address (0:E:0–7)

Bit Number	Bit Name	Description
0	MDA0	Modem Data. When reset by the host, it causes the modem to read/write DPR0:0 (depends on whether RAMWS bit (DPR0:5:5) is "0"–read or "1"–write). It will be reset to 1 after the modem is done. This bit is used for parallel mode as well as for the diagnostic data retrieval.
1		Not used.
2	IE0	Interrupt Enable. When MDA0 bit (DPR0:E:0) is set, IE0 = 1 is the necessary condition to cause the interrupt ($\overline{IRQ}$ = 0).
3	SETUP	Configuration Setup Bit. If set by the host, it causes the modem to reconfigure itself according to the control word specified in the configuration register (DPR0:4), and to assume the options specified for the equalizer (DPR0:5:1), energy detection threshold (DPR0:5:0) and the black pixel extending option in Group 1 FAX operation. This bit returns to zero when acted on by the modem. The time required to complete the reconfiguration depends on the current state of the modem.
4	SHTR	Short Train. In V.27 mode application, if this bit is set by the host, it puts the modem into a fast equalizer training state as defined in CCITT recommendation V.27 ter; if reset, the normal training sequence is followed.
5–6		Not used.
7	IA0	Interrupt Active. This bit is set when the $\overline{IRQ}$ pin is driven to low.

Register 5 Address (0:5:0–7)

Bit Number	Bit Name	Description
0	LRTH	Lower Energy Detect Threshold. LRTH = 1 selects a lower energy detect (ED) threshold. That is, when set, the modem receiver turns on with any incoming signal above -47 dBm instead of the default of -43dBm.
1		Not used.
2	QEXT	Squelch Extended. When set by the host, it will inhibit the modem from RX for 130 msec after the TX turnoff sequence is completed.
3	EPT	Echo Protect Tone. When set, an unmodulated carrier is trasmitted for 185 msec followed by 20 msec of silence at the beginning of the training sequence. This option is available in V.29 and V.27 modes only.
4	RAE	RAM Address. When RAMWS (DPR0:5:5) is set, the one state of this bit selects the XRAM locations; the zero state then selects YRAM locations.
5	RAMWS	RAM Write Extension. This bit should be set if the host is wishing to perform a diagnostic write to chip 0. RAMWS should be reset (RAMWS = 0) when the host is wishing to perform a diagnostic read.
6	TDIS	Training Disable Chip 0. If TDIS is set in the RX mode, the modem is prevented from entering the training phase. If this bit is set prior to $\overline{RTS}$ pin (or RTS bit) is set, there will be no training sequence after line connection.
7	RTS	Request to Send. If set, it signals the modem to start to TX. The modem will continue to TX until this bit is turned off, and the necessary turn-off sequence has been completed. RTS parallels the operation of the hardware $\overline{RTS}$ control pin. These inputs are "OR"ed by the modem.

DUAL PORT RAM MEMORY INTERFACE (BANK 0) (continued)

Register 4 Address (0:4:0–7)

Bit Number	Bit Name	Description
0–7		Configuration. Different modem operation modes are controlled by the host by writing the corresponding control code into this register.

The control codes for the available configurations* are:

A. Facsimile Applications	CONTROL CODE (HEX)
1. V.29 (9600)	14
2. V.29F (7200)	12
3. V.27 (4800)	0A
4. V.27F (2400)	09
5. V.21 FAX	20
6. Group 2*	40
7. Group 1 (1)*	41
8. Group 1 (2)*	42
9. Group 1 (3)*	43
10. Tone mode	80
11. DTMF mode	81
12. Voice Mode	82

CONFIGURATION DEFINITIONS

A. FAX Applications

1 & 2. *V.29.* When a V.29 configuration is selected, the modem operates as specified in CCITT Recommendation V.29. That is, a half duplex communication at 9600 bit/s speed with 16-QAM modulation.

3 & 4. *V.27.* When a V.27 configuration is selected, the modem operates as specified in CCITT Recommendation V.27ter.

5. *FSK (V.21).* In this mode, the modem operates as a CCITT T.30 compatible 300 bit/s FSK modem having the characteristics of the CCITT V.21 channel no. 2 modulation scheme.

6. *Group 2.* The modem operates as a CCITT T.3 compatible modem. This operation, with a simple AM modulation scheme, permits transmission to and reception from Group 2 apparatus. A carrier frequency of 2100 Hz is used. A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black.

7, 8, 9. *Group 1.* In this configuration, the modem operates as a CCITT T.2 compatible FSK modem. Input data is clocked in at a rate of 5184 Hz. To save the bandwidth the black pixels are extended by n trailing pixels, where n = 1, 2 or 3. The corresponding control codes are 41, 42 or 43.

10. *Tone Mode.* In this mode, the modem is able to TX a single frequency as specified by the host. Two registers (DPR0:2 and DPR0:3) are allocated to take in the intended frequency (see FREQL and FREQM).

11. *DTMF Mode.* In this configuration, the activating RTS causes the modem to TX two tones at frequencies and amplitude levels as specified by the user. On the other hand, in the DTMF RX mode (when RTS is deactivated), the modem decodes the incoming DTMF signal and outputs the result in DPR1:A.

12. *Voice Mode.* In this mode, the modem is capable of processing the incoming voice signal or prestored voice message. In voice TX, a 16-bit word is taken in from DPR0:0 (LSB) and DPR0:1 (MSB); in RX, the output can be retrieved in DPR0:0 (LSB) and DPR0:1 (MSB).

In voice transmit mode, a 16-bit word is taken from YSM and YSL (0:0, 0:1). In receive, the data can be retrieved from the same location. See transceiver data.

* Not necessarily available to all data pump kits; refer to data book for detail.

DUAL PORT RAM MEMORY INTERFACE (BANK 0) (continued)

Register 4 Address (0:4:0–7)

Bit Number	Bit Name	Description

Register 3 Address (0:3:0–7)

Bit Number	Bit Name	Description
0–7	XSM	RAM DATA. RAM location RD/WR by the host (most significant byte of word X).

Register 2 Address (0:2:0–7)

Bit Number	Bit Name	Description
0–7	XSL	RAM DATA. Chip 0 RAM location RD/WR by the host (least significant byte of a 16 bits word X).

Register 1 Address (0:1:0–7)

Bit Number	Bit Name	Description
0–7	YSM	RAM DATA. RAM location RD/WR in chip 0 by the host (most significant byte of word Y).

Register 0 Address (0:0:0–7)

Bit Number	Bit Name	Description
0–7	YSL	RAM DATA. The least significant byte location of RAM location read/write (RD/WR) of a 16 bit word Y by the host in chip 0. This register also shared by parallel mode operation (TX/RX) for passing data between host and modem. See DPR0:0 and bit MDA0 for detail. In receive (RX) parallel mode, the modem presents 8 bits of received data in this register to pass to the host processor. Moreover, the modem sets MDA0 bit (DPR0:E:0) to one to signal the availability of data. After the host reads register 0:0, it should reset bit MDA0. Also, the first received data is not necessarily located in bit 0:0:0. The host must frame the received data by searching for message sync character. Data available flag (MDA0) sets at one eighth the bit rate in parallel data mode rather than at the sample rate at it does when reading RAM location. In transmit (TX) parallel mode, the host also puts data at this location 8 bits at a time and clears MDA0 bit (MDA0 = 0). After modem moves the 8 bit data in, it sets MDA0 back to 1 to prompt the host for the next set of data.

DUAL PORT RAM MEMORY INTERFACE (BANK 1)

Register F Address (1:F:0–7)

Bit Number	Bit Name	Description
0–7		RAM Access. This register is the interface buffer for the RAM access code used by the host in reading from or writing to the RAM locations in bank 1.

Register E Address (1:E:0–7)

Bit Number	Bit Name	Description
0	MDA1	Modem Data Available (Bank 1). To write to bank 1, the host needs to set this bit; it should reset this bit after a read cycle.
1	AUDIO	Audio Output Control. If set, the RX input signal is routed to the AUDIO OUT pin; when reset, the AUDIO OUT pin is disabled. If this bit is set, it is recommended to set the RX0 bit also, to disable the RX input.
2	IE1	Interrupt Enable. When MDA1 is set (DPR1:E:0), IE1 = 1 indicates the $\overline{IRQ}$ pin is being driven to low.
3–4	TX1–TX0	Transmit Section. TX output signal can be controlled by these two bits according to the following spec:

TX1	TX0	Signal at TXOUT Pin
1	1	Squelch TX
0	0	TX signal from attenuator
0	1	AUXTX signal
1	0	Both of the above

5		Not used.
6	EYE/TX	Eye/Normal Mode. EYE/TX = 1 puts the D/A converter in the eye pattern monitor mode; EYE/TX = 0, the D/A converter then serves the TX needs.
7	IA1	Interrupt Active. If set, chip 1 drives $\overline{IRQ}$ to low.

Register D Address (1:D:0–7)

Bit Number	Bit Name	Description
0	RAMWB	RAM Write Bank 1. When the host performs a diagnostic write, it should set this bit; for a diagnostic read, the host should then reset this bit.
1	FRT	Freeze Taps. If set, the adaptive equalization taps are frozen. That is, all tap values stay fixed and no more tap adjustment. If reset (FRT = 0), the adaptive algorithm resumes function.
2–7		Not used.

Register C Address (1:C:0–7)

Bit Number	Bit Name	Description
0		Not used.
1–4	TL3–TL0	Transmit Level . These 4 bits control a 15 step programmable attenuator with 1 dB per step. The amount of attenuation corresponding to each bit is as follows:

TL3	TL2	TL1	TL0	Attenuation (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	1	0	0	4
1	0	0	0	8

5	FDEN	Flag Detector Enable. If set by the host, the HDLC flag detector is enabled. The result (whether there is a valid detection) is put in the FLAG bit (DPR1:7:5).

DUAL PORT RAM MEMORY INTERFACE (BANK 1) (continued)

Register C Address (1:C:0–7)

Bit Number	Bit Name	Description
6	SETUP2	Setup 2. If set by the host, it causes the modem to reconfigure the analog section as specified by the host, and to assume whatever the options specified by the host regarding the eye pattern control (DPR1:E:6), RX section input control (DPR1:C:7), TX section output control (DPR1:E:3-4), and TX level control (DPR1:C:1-4). This bit resets to zero when acted on by the modem.
7	RXO	Receive Section Input Control. If set, it indicates the analog input signal is ground; if reset (RX0 = 0), the received input signal is taken in from the line.

Register B Address (1:B:0–7)

Bit Number	Bit Name	Description
1–4		Not used.
5–7	FR3–FR1	Frequency Detection. The contents of these three bits indicate the reception of three different tonal signals respectively: FR3 = 1 462Hz FR2 = 1 1100Hz FR1 = 1 2100Hz

Register A Address (1:A:0–7)

Bit Number	Bit Name	Description
0–6	COL3–COL1 ROW4–ROW1	DTMF Detect. The contents of this register indicate the results of DTMF detection.

	COL1	COL2	COL3
ROW1	1	2	3
ROW2	4	5	6
ROW3	7	8	9
ROW4	*	0	#

7		Not used.

Register 7 Address (1:7:0–7)

Bit Number	Bit Name	Description
0	$\overline{\text{CDET}}$	Carrier Detected. $\overline{\text{CDET}}$ = 0 flags the host of the completion of the training sequence. That is, $\overline{\text{CDET}}$ goes to zero at the beginning of the data state. This bit activates up to 1 symbol time before the $\overline{\text{RLSD}}$ and deactivates within 2 symbol times after $\overline{\text{RLSD}}$ changes.
1–3		Not used.
4	RINGIN	Ringing Input. The state of this bit represents the state of the signal applied to the RINGIN pin after passing the debounce circuit.
5	FLAG	HDLC Flag. If FDEN (DPR1:C:5) is set, FLAG = 1 indicates a valid HDLC flag has been detected.
6	$\overline{\text{PNDET}}$	Period 'N' Detection. This bit will be clear when the PN sequence as defined in CCITT V.29 is detected. It will be reset ($\overline{\text{PNDET}}$ = 1) as PN sequence finished.
7		Not used.

Register 5 Address (1:5:0–7)

Bit Number	Bit Name	Description
0	PD	Power Down Enable. If set by the host, it forces the modem to get into the power down (energy saving) mode until this bit is reset by the host again. This bit only works on those chips equipped with power down capability.
1–5		Not used.

DUAL PORT RAM MEMORY INTERFACE (BANK 1) (continued)

Register 5 Address (1:5:0–7)

Bit Number	Bit Name	Description
6	$\overline{\text{FED}}$	Fast Energy Detect. $\overline{\text{FED}}$ = 0 indicates the incoming signal is above the preset passing band energy threshold.
7		Not used.

Register 4 Address (1:4:0–7)

Bit Number	Bit Name	Description
0		Not used.
1	CTSP	Clear To Send Parallel. When set, it flags the DTE that the training sequence is completed and any data present at TXD pin will be TX by the modem. The status of this bit parallels the $\overline{\text{CTS}}$ pin.
2	$\overline{\text{P2DET}}$	Period '2' Detection. When clear, it indicates the second training period symbol as defined in CCITT V.29 is detected.
3–5		Not used.
6	RDREN	Reduced Voice Rate Enable. If RDREN is set in VOICE mode, the voice sample rate is reduced from 9600 bit/sec to 4800 bit/sec.
7	MUEN	MU Law Enable. When set in VOICE mode, the mu law compression/decompression algorithms are activated. In RX mode, the 10 bits A/D samples are compressed to 8 bits; in TX, the compressed 8-bit data is decompressed to 10-bit before being sent to the D/A.

Register 3 Address (1:3:0–7)

Bit Number	Bit Name	Description
0–7		RAM Data XBM. MSB of a 16-bit word X used in the RD RAM location in bank 1.

Register 2 Address (1:2:0–7)

Bit Number	Bit Name	Description
0–7		RAM Data XBL. LSB of a 16-bit word X used in the RD RAM location in bank 1.

Register 1 Address (1:1:0–7)

Bit Number	Bit Name	Description
0–7		RAM Data YBM. MSB of a 16-bit word Yused in the RD/WR RAM location in bank 1.

Register 0 Address (1:0:0–7)

Bit Number	Bit Name	Description
0–7		RAM Data YBL. LSB of a 16-bit word Y used in the RD/WR RAM location in bank 1.

PERFORMANCE

Whether functioning in V.27 ter or V.29 configuration, the modem provides the user with unexcelled high performance.

Typical Bit Error Rates

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of -20 dBm as illustrated.

Typical Phase Jitter

At 2400 bit/s, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of a 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of a 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bit/s (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 21 dB in the presence of a 15° peak-to-peak phase jitter at 300 Hz.

At 7200 bit/s (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of a 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bit/s, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 26 dB in the presence of a 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 26 dB in the presence of a 20° peak-to-peak phase jitter at 30 Hz.

The BER curves shown were prepared from data obtained using a PTT communication test system.

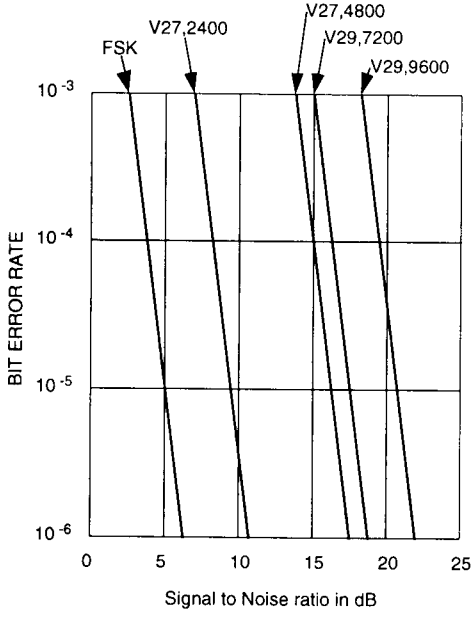


Figure 3.
Typical Bit Error Rate
(Back-to-Back, T/2 Equalizer, Level -20 dBm)

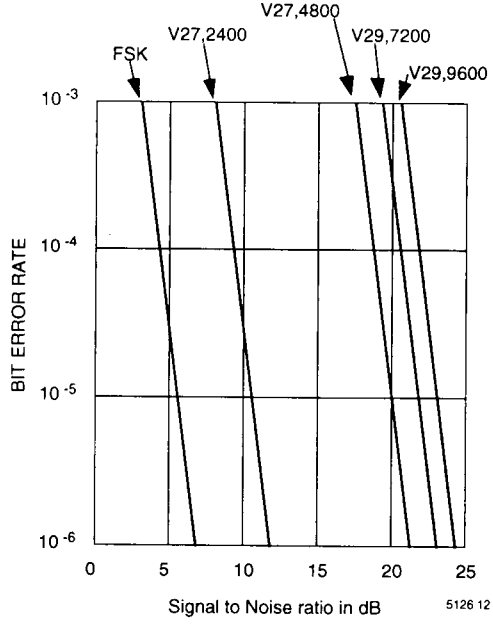


Figure 4.
Typical Bit Error Rate
(Unconditioned 3002 Line, T/2 Equalizer, Level -20 dBm)

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage	+6 V
Input Voltage	-0.6 V to V_{CC} + 0.6V
Storage Temperature Range	-65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	0 to 70°C

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = +5 V ± 10%)

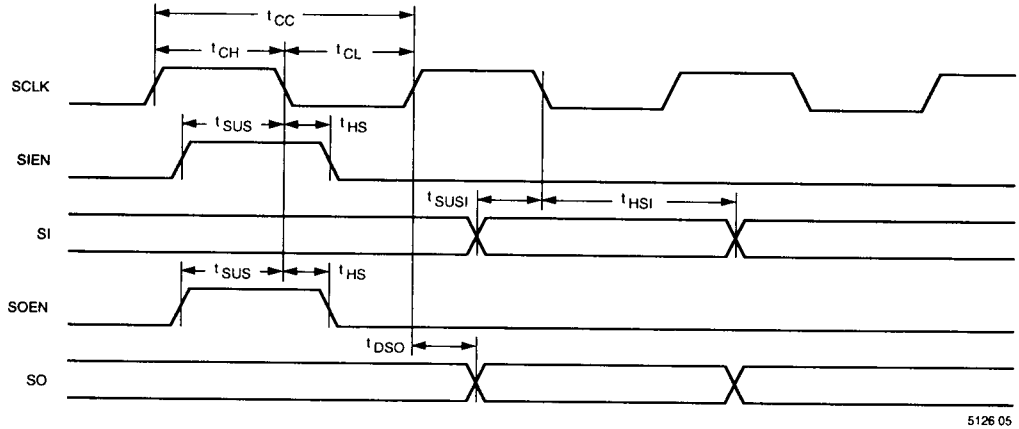
PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC}	Nominal Operating Current @ V_{CC} = 5.5V		40	90	mA
I_{CC}	Power Down mode		12	25	mA
F_{CLK}	Crystal Clock Frequency	19.6589	19.6608	19.6627	MHz

DIGITAL INTERFACE CHARACTERISTICS (DC)

Symbol	Parameter	Units	IA	IB	IC	ID	IE	OA	OB	OC	I/OA	I/OB
V_{IH}	Input High Voltage	V	2.0min	3.15min	2.0min	2.0min	3.15min				2.0min	2.0min
V_{IL}	Input Low Voltage	V	0.8max	1.35max	0.8max	0.8 max.	1.35max				0.8max	0.8max
V_{OH}	Output High Voltage	V							3.65min[1]	3.65min[1]	2.4min[1]	2.4min[3]
V_{OL}	Output Low Voltage	V						0.4max[2]	0.85max[2]	0.85max[2]	0.4max[2]	0.4max[2]
I_{OH}	Output High Current	mA							-0.1	-0.1		
I_{OL}	Output Low Current	mA						1.6	1.6	1.6		
IPU	Short Circuit Pullup Current	µA			-240max -100min		-240max -100min	-240max -100min				-240max -100min

NOTE 1: I_{LOAD} = -100 µA
NOTE 2: I_{LOAD} = 1.6 mA
NOTE 3: I_{LOAD} = -40 µA

SIO PORT TIMING



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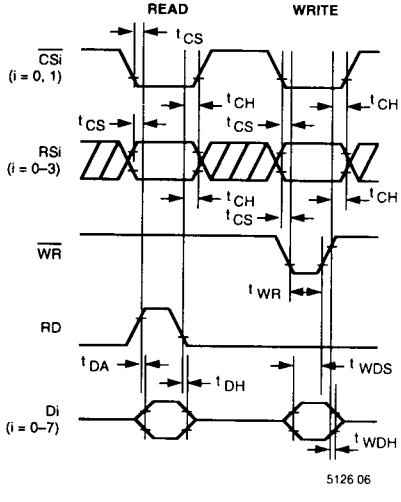
PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
t_{CC}	SCLK Cycle Time		408		ns
t_{CH}	SCLK High Pulse Width*		204		ns
t_{CL}	SCLK Low Pulse Width*		204		ns
t_{SUS}	SIEN/SOEN setup before SCLK falling	50			ns
t_{HS}	SIEN/SOEN hold time after SCLK falling	100			ns
t_{SUSI}	SI setup before SCLK falling	50			ns
t_{HSI}	SI Hold time after SCLK falling	50			ns
t_{DSO}	SO Valid after SCLK rising			100	ns

*Duty Cycle Must Be Within 40-60%

MICROPROCESSOR INTERFACE TIMING DIAGRAM



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CRITICAL TIMING REQUIREMENTS

PARAMETER	CHARACTERISTIC	MIN	MAX	UNITS
t_{CS}	$\overline{CSi}$, RSi setup time prior to Read or Write	30	—	ns
t_{DA}	Data Access time after Read	—	140	ns
t_{DH}	Data hold time after Read	10	50	ns
t_{CH}	$\overline{CSi}$, RSi hold time after Read or Write	10	—	ns
t_{WDS}	Write data setup time	75	—	ns
t_{WDH}	Write data hold time	10	—	ns
t_{WR}	Write strobe pulse width	75	—	ns