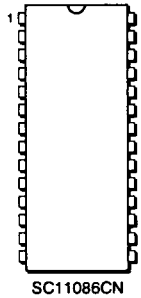
FEATURES

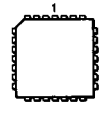
- ☐ SC11086 Supports CCITT Group 3 Facsimile
- ☐ SC11196 Supports CCITT Groups 1, 2 & 3 Facsimile
- ☐ Internal Hybrid for 2-wire PSTN
- ☐ Direct Interface to SC11006, SC11026 MAPs
- ☐ Compatible with CCITT V.29, V.27ter, V.21 channel 2
- ☐ Cable compensation selectable
- ☐ Internal constellation pattern DACs
- ☐ Ring Detector Input
- ☐ Dynamic Range -47dBm to 0dBm
- ☐ Programmable transmit levels to +5dBm ±1dB
- ☐ Power consumption 190mW
- ☐ 10 bit ADC & DAC voice band sampling

28-PIN DIP PACKAGE



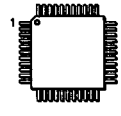
SC11086CN
SC11196CN

28-PIN PLCC PACKAGE



SC11086CV
SC11196CV

44-PIN QFP (10mm) PACKAGE



SC11086CQ
SC11196CQ

GENERAL DESCRIPTION

The SC11196 and SC11086 are Facsimile Modem Analog Processors (FMAP) designed to work with Sierra's SC11198 series DSP ICs to form a 9600 bps data pump. The combination of FMAC and DSP provides a register compatible replacement for the Rockwell 96MD fax data pump. The chipset offers several advantages including internal hybrid, DTMF detection, voice mail modes, direct line drive for dial up applications and a variety of packaging options. These chipsets can also be combined with Sierra data modem kits to form EIA Class 2 fax and data modems supporting the developing standard PN2388 command set as well as

BLOCK DIAGRAM

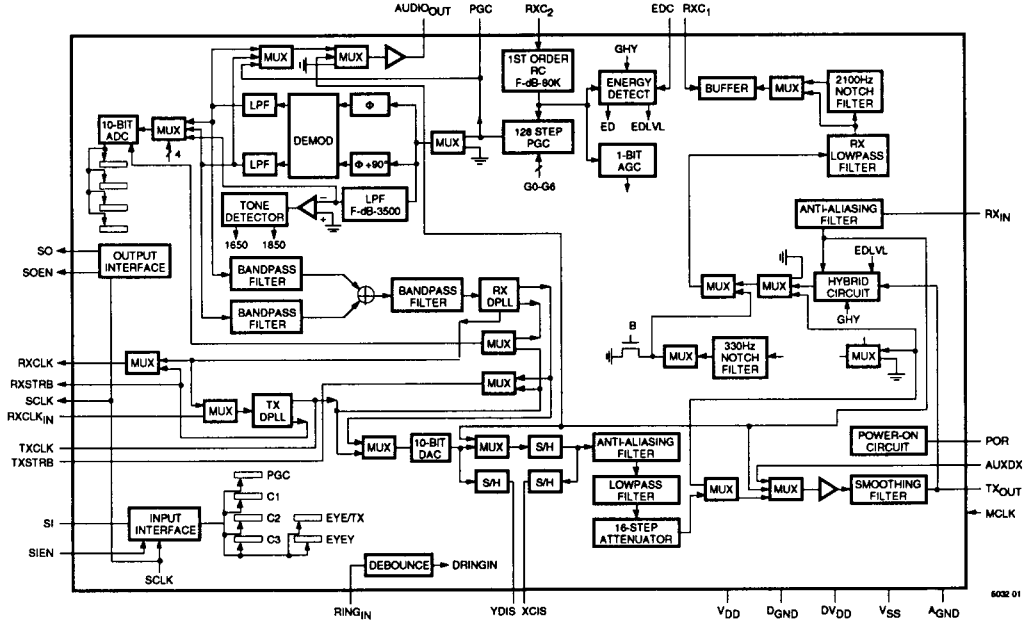


Figure 1.

GENERAL DESCRIPTION (continued)

AT commands for data modems. Versions to support V.42bis, MNP5 and other protocols are available. Please consult the SC11198 series data sheet for further details of the fax data pump.

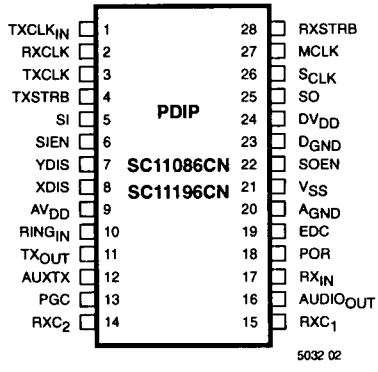
PIN DESCRIPTIONS

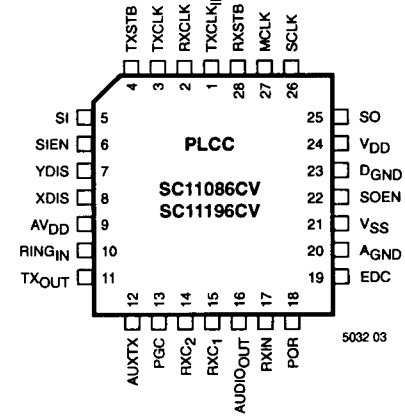
PIN NAME	PIN NUMBER DIP, PLCC	PIN NUMBER QFP	TYPE	DESCRIPTION
A_{GND}	20	27	P	Analog ground input; A_{GND} = 0V.
$AUDIO_{OUT}$	16	18	O	Audio signal output (analog). The receive signal is passed through a unit gain buffer which can drive 10KΩ resistive load. It drives an external gain amplifier to drive a speaker for line monitoring.
AUXTX	12	13	I	Auxiliary transmit signal input (analog). It can be summed up with the transmit signal or it can be sent directly to the TXOUT pin.
AV_{DD}	9	8	P	Analog positive power supply input; AV_{DD} = +5V ±10%.
D_{GND}	23	31	P	Digital ground input; D_{GND} = 0V.
DV_{DD}	24	32	P	Digital positive power supply input; DV_{DD} = +5V +±10%.
EDC	19	24	O	Energy detect capacitor input (analog). An external 0.47µF capacitor should be connected between this pin and A_{GND} pin.
MCLK	27	38	I	Master clock input (TTL compatible). Its frequency must be 9.792MHz. This clock is used to generate various timing signals for internal and external use.
PGC	13	14	O	Programmable Gain Control (PGC) output (analog). It is a sampled and held analog signal. It can drive a 10KΩ resistive and 50pF capacitive load.
POR	18	20	O	Power-on-reset output (TTL compatible) with the clock running. A negative pulse of 36 msec will be generated on power-on when the power supply voltage V_{DD} exceeds 3.75V. This pin will remain high until V_{DD} drops below 3.0V for 35msec.
$RING_{IN}$	10	10	I	Ringin input (analog). Ringin tone is input to a debouncer circuit that has a lower threshold voltage at 2.2V and a upper threshold voltage at 2.8V with 600mV hysteresis. A voltage at Ringin higher than 2.8V will force the DRINGIN bit of output register to high while lower than 2.2V will force it low.
RXC_1	15	17	O	Receive filter output (analog). It can drive a 10KΩ resistive load. An external 0.1µF AC coupling capacitor is required to connect the RXC1 and RXC2 pins. This capacitor together with an internal 20KΩ resistor forms a high-pass filter that removes the DC offset from the receive signal before entering the PGC.
RXC_2	14	16	I	PGC input (analog). It is the PGC input and has an internal 20KΩ resistor to ground.
RXCLK	2	42	O	Receive bit clock output (TTL compatible). In V.29, V.27, V.33 modes, the falling edge of RXSTRB is synchronous to the rising edge of RX_{CLK}. In other modes (i.e. FSK, V.21 mode, G2/G1 mode and tone generation) the RX_{CLK} is the same as RXSTRB.
RX_{IN}	17	19	I	Receive signal input (analog). It has a nominal input impedance of 65KΩ.
RXSTRB	28	39	O	Receive strobe clock output (TTL compatible). In V.33, V.29 and V.27 modes, it is synchronous to the recorded band clock. It is a negative pulse with periods of 6.9msec to 13.8msec in various modes. It is used as an interrupt signal to the DSP chip. In each RXSTRB period, four samples taken from the receive I and Q channels and converted into digital data and shifted out serially. In other modes, RXSTRB is the same as TXSTRB and only one sample of the received signal per RXSTRB period is taken and converted into digital data and shifted out to the DSP.

PIN DESCRIPTIONS (CONTINUED)

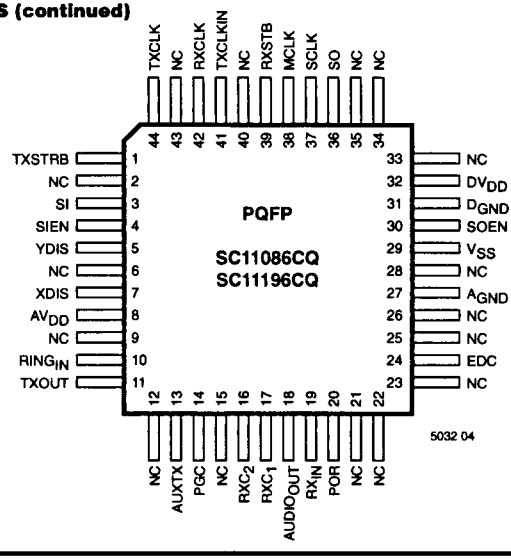
PIN NAME	PIN NUMBER DIP, PLCC	PIN NUMBER QFP	TYPE	DESCRIPTION
S_{CLK}	26	37	O	Shift clock output (TTL compatible). Its frequency is 1/4 of MCLK. Its duty cycle is 50%. It is used for serially shifting both transmit and receive data in and out of the chip.
SI	5	3	I	Serial data input (TTL compatible). Input data is shifted serially into a 13-bit register by using the falling edge of S_{CLK}. The three most significant bits (D12-D10) address the contents of 10 least significant bits (D9-D0) into data/control register. The MSB is shifted in first.
SIEN	6	4	I	Serial enable input (TTL compatible). It enables the writing of serial data into the 13-bit input register.
SO	25	36	O	Serial data output (TTL compatible). Output 16 bit data is shifted out serially by using the rising edge of SCLK. The ten most significant bits (D15-D6) correspond to the ADC output data. The next five bits (D5-D1) correspond to various status bits, such as D5 corresponds to ED output, D4 to AGCG output, D3 to DRINGIN output, D2 to 1650Hz tone detected and D1 to 1850Hz tone detected. The LSB (D0) is a don't care.
SOEN	22	30	O	Serial enable output (TTL compatible). A positive pulse enables the 16 bit data stored in a receive shift register to be read out serially through the SO pin.
TXCLK	3	44	O	Transmit bit clock output (TTL compatible). It is synchronous to the TX_{CLKIN} in the external clock mode. In the free run (internal) mode it is derived from the crystal clock.
$TXCLK_{IN}$	1	41	I	External transmit clock input (TTL compatible). It is for the input clock of the transmit phase-locked loop.
TXSTRB	4	1	O	Transmit strobe clock output (TTL compatible). It is used to interrupt the DSP to transfer transmit eye-x/eye-y or control data. In G2/G1 mode TXSTRB is 10.368kHz. It is 9600Hz in all other modes.
TX_{OUT}	11	11	O	Transmit signal output (analog); It can drive a 600Ω resistive load directly.
V_{SS}	21	29	P	Negative power supply input; V_{SS} = -5V ± 10%.
XDIS	8	7	O	Eye-X display output (analog); 10 bits D/A output from Eye-X register.
YDIS	7	5	O	Eye-Y display output (analog); 10 bits D/A output from eye-Y register. Both X and Y data word are written into the chip within a given strobe period and they will appear simultaneously at XDIS and YDIS two strobes later.

CONNECTION DIAGRAMS





CONNECTION DIAGRAMS (continued)



SC11086 FUNCTIONAL DESCRIPTION

Generally, when implementing a system, such as a modem, there is a chip size tradeoff between the analog signal processor (ASP) and the digital signal processor (DSP). In its simplest form, the ASP for a modem consists of a band-pass filter, a programmable gain control (PGC) and an analog-to-digital converter (ADC) for the receiver; and a digital-to-analog converter (DAC) and a transmit filter for the transmitter. In such an arrangement the analog signal is normally sampled at 9600Hz, and the samples are transferred to the DSP chip. The DSP chip performs signal processing at the sample rate to demodulate the signal. In another arrangement, switched-capacitor design techniques can be used to further process the passband signal in the analog domain and recover the baseband signal and the baud timing. The baseband signal is subsequently sampled at the baud rate and the samples are transferred to the DSP chip. In this case, the signal processor operates at the baud rate, which is normally several times slower than the sample rate, hence making the design of the DSP chip and the software development much easier.

The SC11086 Fax Modem Analog Signal Processor (ASP) is designed for a modem system based on the latter approach. It recovers the in-phase and quadrature components of the baseband signal, samples it at the baud rate (or twice the baud rate) and transfers it to the DSP chip. The DSP performs the rest of the demodulation which includes adaptive equalization, carrier tracking, derotation and descrambling. The two chip system is shown in Figure 1. The data transfer between the DSP and analog chip is performed through a serial port. The DSP chip also communicates with a controller on an 8-bit microprocessor bus.

System Architecture

The block diagram of the ASP is shown in Figure 1. The receive signal, after passing through an antialiasing filter, is applied to a hybrid circuit and a one-bit automatic gain control (AGC). The AGC is followed by the receive filter and a smoothing low-pass filter, which removes the clock components from the output signal. Subsequently the signal is AC coupled to a 512 step 0.1dB/step programmable gain control (PGC). The PGC, under the control of the DSP chip, amplifies the receive signal before it is applied to the demodulator. The demodulator consists of a Hilbert transformer which splits the signal into two components that are 90 degrees out of phase with respect to each other. The two signals are multiplied by the sine and cosine of a free running carrier, demodulated and filtered to recover the baseband in-phase (I) and quadrature phase (Q) components of the signal. The baseband I and Q signals are used in the clock recovery circuit to recover the timing signal. The output of the timing recovery has a substantial amount of jitter, which is removed by a digital phase-lock loop. The timing signal is then used to take two samples from the baseband I and Q signals, one in the middle of the baud (Im and Qm, midbaud) and one at the end of the baud (Ie and Qe, endbaud). The four baseband signal samples are converted into a 10-bit digital word by a successive approximation ADC and stored in four registers. The recovered baud timing is also brought out of the chip and is used as the receive interrupt to the DSP chip. The output interface

circuit, under the control of the baud timing, transfers the the four baseband samples the DSP chip through a serial interface. The DSP chip uses the samples to demodulate the data by a T/2 (T is the baud period) or T-spaced adaptive equalizer.

On the transmit side, the complete modulation function is implemented in the DSP chip. Under the control of the (9600Hz) transmit strobe, the DSP chip transfers one transmit sample to the ASP through the serial input interface. The transmit sample is converted to analog by a 10-bit digital-to-analog converter and is subsequently filtered by the transmit low-pass filter to remove the high frequency components. The transmit signal passes through a 15-step, 1dB/step attenuator before it is applied to the transmit pin. Several other auxiliary functions such as energy detect circuit; X and Y eye DACs; power-on reset and analog loopback are also implemented on the chip. In the next sections the major blocks of the chip will be described.

Receive Section

Hybrid and One Bit Automatic Gain Signal

The receive signal first goes through an antialiasing filter (AAF) to remove the high frequency components, which will otherwise be aliased into the baseband due to the sampling effects of the receive filter. The receive signal then goes through a hybrid circuit and a one bit automatic gain control (AGC). The hybrid function is necessary when the chip works in full-duplex (FDX) applications, such as the G2 facsimile mode, where the receiver has to detect the presence of a far end signalling tone while it is transmitting the modulated signal. The hybrid/AGC shown in Figure 2 cancels the transmit signal by summing the receive input signal with one-half of the transmit signal with a reverse polarity. The one bit AGC periodically monitors the peak of the signal over 4msec intervals to set the AGC gain in such a way that the peak of the signal falls within a predefined window. If the level of the input signal is weak, the gain will be 12dB, otherwise 0dB. The hybrid can also be used to connect a data modem through an auxiliary input.

The 1-bit AGC adjusts the gain based on the peak of the signal. It turns off when the signal exceeds 1.6V, and turns on when the signal falls below 150mV. The receive input signal is amplified by 12dB in the hybrid as soon as the 1-bit AGC turns on. Normally, after the initial handshake, the upper threshold of the AGC is increased to 2.5V to prevent the gain from changing due to gain hits.

Receive Filter

The receive filter is shown in Figure 2 in block diagram form. The first section is a low-pass switched-capacitor ladder filter. The filter has a 3.3KHz bandwidth with 0.1dB passband ripple; the minimum stopband rejection is 51.5dB. Following the low-pass filter is a bypassable switched-capacitor low-pass filter with a notch at 2100Hz. This filter can be inserted in the receive signal path when the modem is transmitting in the FAX G2 mode and the receiver concurrently detects the presence of a signalling tone in the range of 300-1100Hz. The notch frequency is set to 2100Hz, which is the same as the G2 mode carrier frequency. The output of the receiver lowpass or the 2100Hz notch filter then passes through a highpass filter followed by a smoothing filter to drive an external AC coupling capacitor with an internal resistor.

Programmable Gain Control (PGC)

The external capacitor and the internal resistor form a high-pass filter that removes the DC component of the filtered signal before entering the PGC. The PGC has a wide range of 51.2dB and can be programmed externally by the DSP chip in 512 steps, 0.1dB/step, through a 9-bit control signal.

The PGC circuit is composed of four AC coupled switched-capacitor gain stages. The gain of the PGC is varied by the signal processor under the control of the software AGC loop. The demodulation process in the modem cannot tolerate any transient behavior when the PGC gain is altered. Therefore, the PGC resets itself every clock cycle and cancels its DC offset successively through four AC coupled stages to amplify the input signal. This process allows the gain to be changed from one cycle to the next by any amount without causing any transient effects. The first two stages of the PGC give the macro gains of 0, 12.8, 25.6, and 38.4dB controlled by the two most significant bits (MSBs). The third stage gives the gain adjustment of 0, 3.2, 6.4 and 9.6dB controlled by the next two significant bits. The last stage gives the macro gain adjustment of 0–3.1dB with 0.1dB/step, controlled by the remaining five bits.

Demodulator

In a "two dimensional" signal system, two independent variables, a(t) and b(t), are used to transmit data. The incoming data stream in the transmitter is encoded by the line coder into the two streams a(t) and b(t). Then a(t) is modulated by $\cos(\omega t)$ and b(t) is modulated by $\sin(\omega t)$, where $f = \omega/2\pi$ is the carrier frequency. The results are added to give the transmitted signal

$$x(t) = a(t) \cdot \cos(\omega t) + b(t) \cdot \sin(\omega t)$$

Since the sine and cosine functions are 90 degrees out of phase, or in quadrature, hence the name quadrature amplitude modulation, or QAM.

In the receiver, a(t) and b(t) are recovered by multiplying the incoming signal, x(t) by the cosine and sine of the carrier, resulting in the lowpass baseband components and

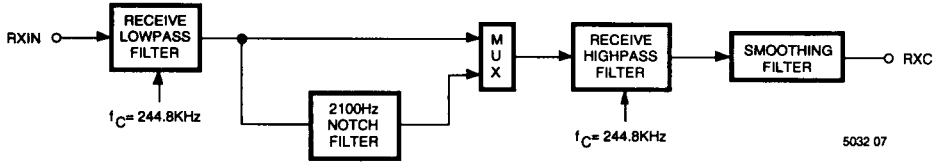


Figure 2. Receive Filter in Block Diagram Form

components centered at 2fc, which can be removed by lowpass filtering. A more efficient way to eliminate the 2fc sideband is to use a single-sideband (SSB) demodulator. In exact analogy to the SSB demodulator, we can recover a(t) and b(t) from an appropriate combination of the in-phase and quadrature receive signals, as shown in Figure 3.

The phase-shifter in Figure 3, also known as a Hilbert transformer, produces an in-phase and 90 degrees out of phase component over the frequency band of the receive signal. The output of the PGC goes to the demodulator. In the demodulator, the signal first passes through the Hilbert transformer that produces in-phase and 90 degree out-phase components.

The in-phase and the out-phase components from the output of the Hilbert transformer are then demodulated to the baseband in a mixer stage. This is achieved by multiplying the individual components by a free-running carrier. The frequency of the carrier is 1700Hz for V.29 mode and 1800Hz for V.27ter. The block diagram of the QAM modulator is shown in Figure 3. The baseband components are filtered by two lowpass filters with -3dB frequencies equal to one-half of the baud frequency to produce in-phase (I) and quadrature (Q) channel outputs. The I and Q channel outputs are both smoothed by the distributed R-C filters before they are applied to the 10-bit analog-to-digital converter (ADC), where they are sampled by the recovered timing signal.

The timing recovery circuit is based on filtering the band edge component of the I and Q baseband signals. In this method the band edge component is rectified and filtered by a bandpass filter centered at the baud rate to recover the timing signal. To optimize the chance of recovering the timing information both inphase and quadrature components are used, since one may carry an AC signal, while the other happens to be temporarily DC. Therefore, first the I and Q signals are passed through two bandpass filters centered at half the baud rate to recover the band edge components. Subsequently the band edge components are rectified and summed before they are applied to a bandpass filter with a center frequency equal to the baud rate. The output of the bandpass filter is sliced to give the raw baud clock. This signal has a substantial amount of jitter, which is removed by applying it to a digital phase lock loop (DPLL), the output of which provides the baud rate clock and the ADC strobes.

Using the ADC strobe, the smoothed I and Q outputs are sampled and converted into 10-bit digital data by the ADC. In the V.29 and V.27ter modes, each channel (I and Q) is sampled twice during a baud cycle, once at the middle and once at the end of the baud period. The external DSP is interrupted by the baud clock. The DSP reads the I and Q samples and performs adaptive equalization, carrier phase tracking, data decoding and data descrambling. In the FSK and tone modes, the ADC strobe is replaced by a 9.6KHz free running strobe, while the ADC input signal is taken from the output of the PGC after passing through a lowpass smoothing SC filter with a cutoff frequency equal to 3500Hz. In the G2 and G1 modes, the strobe frequency is 10.368KHz.

Energy Detector

The energy detector is set to turn on when the signal exceeds -43dBm and turn off when the signal falls below -48dBm. A minimum hysteresis action of 2dB exists between the off-to-on and on-to-off transition levels.

The basic block of the energy detector is shown in Figure 4. The operation of the circuit is as follows. First the signal is amplified and the DC is removed by the highpass SC filter with some gain. Next, the signal is rectified and filtered by a lowpass SC circuit. The output goes to an RC filter, made of an internal resistor and an external capacitor, which removes the AC components, leaving the DC of the signal. The extracted DC, which is equivalent to the energy of the receive signal, is compared to a threshold voltage to detect the energy.

Transmit Functions

Most of the transmit function, which includes data encoding, baseband filtering, and modulation by the quadrature carriers, is performed in the DSP chip. The DSP chip uses the 9600Hz transmit strobe, which is generated by the transmit DPLL in the analog chip, as a time base. On the occurrence of each transmit strobe one 10-bit transmit digital sample is transferred to the analog chip through

the serial interface. The digital-to-analog converter (DAC) in the analog chip converts the 10-bit digital sample to analog, filters it with a switched-capacitor low-pass filter and passes it through a 16 step 1dB/step programmable attenuator before it applies it to the output buffer. The transit section also provides several other functions, such as analog loopback, auxiliary transmit input and auxiliary DAC function for eye pattern monitoring.

10-Bit DAC

The transmit strobe, generated from the transmit DPLL, starts the transfer of a 10-bit digital transmit sample from the DSP to the analog processor. The 10-bit DAC converts the digital sample to an analog value.

The operation of the 10-bit DAC is based on an SC gain stage with a fixed capacitor in the feedback, a programmable capacitor array at the input and a reference voltage as an input source.

The 10-bit DAC can also be used to convert the I and Q digital baseband transmit or receive signals. The analog outputs of these two signals are sampled-and-held and can be displayed simultaneously as eye patterns for the transmit or receive signal constellation.

Transmit Filter

Before going into the transmit filter, the sampled-and-held output of the 10-bit DAC goes through a second-order RC-active filter. This filter is to reduce the aliasing effects between the DAC and the transmit filter that can have asynchronous sampling frequencies.

The transmit filter is a lowpass SC ladder filter. It has a cosine function in the input stage. This doubles the effective sampling frequency of the input signal and hence allows the cutoff frequency of the anti-aliasing filter to be higher; that is, the RC area is smaller. The passband of the transmit filter also has x/sin(x) shape to compensate the loss distortion due to the 9600Hz sample-and-held effect of the DAC.

16-Step Attenuator and the Smoothing Filter

The transmit filter is followed by an SC attenuator. It is a lowpass SC filter, which can be programmed to attenuate the output signal by 0-15dB with 16 steps, 1dB/step. The pass-band edge of the low-pass filter is selected to be high enough so that it will have a negligible effect on the passband of the transmit filter. The SC attenuator has the interpolated output. This reduces the requirements of the smoothing filter that follows it. The smoothing filter is a RC active filter, which can drive a 600Ω load.

Other Features

The chip contains several other features which include a power-on reset and low voltage detector circuit, an audio monitor which passes the receive signal through a 600Ω buffer to drive a speaker, a 1650/1850Hz detector that can be used for HDLC flag detection and a receive digital phase locked loop for receive timing recovery.

Constellation Display

Figure 6 shows the signal constellation for a 16 point 9600 bit/s modem based on the CCITT V.29 standards. The receive signal level was -25dBm with 25dB signal-to-noise ratio and the receive signal passing through a 3002 worst case line simulator. The display of the signal constellation was achieved by feeding the output of the adaptive equalizer from the DSP chip to the eye display monitor of the analog chip.

Summary and Conclusions

The Analog Signal Processor SC11086/SC11196 includes all the necessary signal processing blocks to recover the inphase and quadrature components of the receive baseband signal. It also recovers the baud clock and uses it to sample the baseband components twice in a baud period. The samples are transferred to a companion DSP chip which performs the remaining signal processing functions. Since the baseband signal and baud clock are recovered in the analog chip, the DSP chip operates at the baud rate, allowing it to have a much simpler architecture. The combination of the analog and DSP chips offers the ability to do modulation and demodulation for modems based on the CCITT standards, V.29, V.27ter, V.21 and G2 facsimile modes.

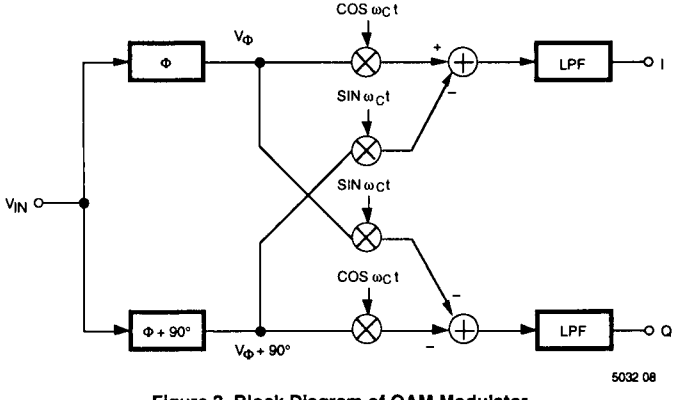


Figure 3. Block Diagram of QAM Modulator

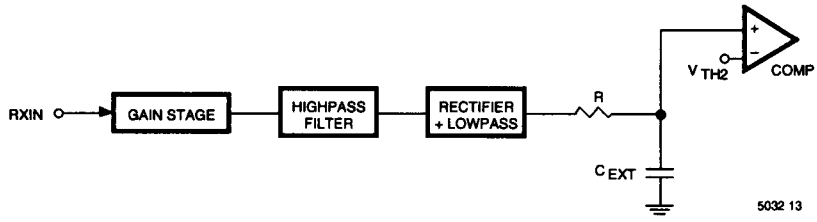


Figure 4. Basic Block Diagram of Energy Detector

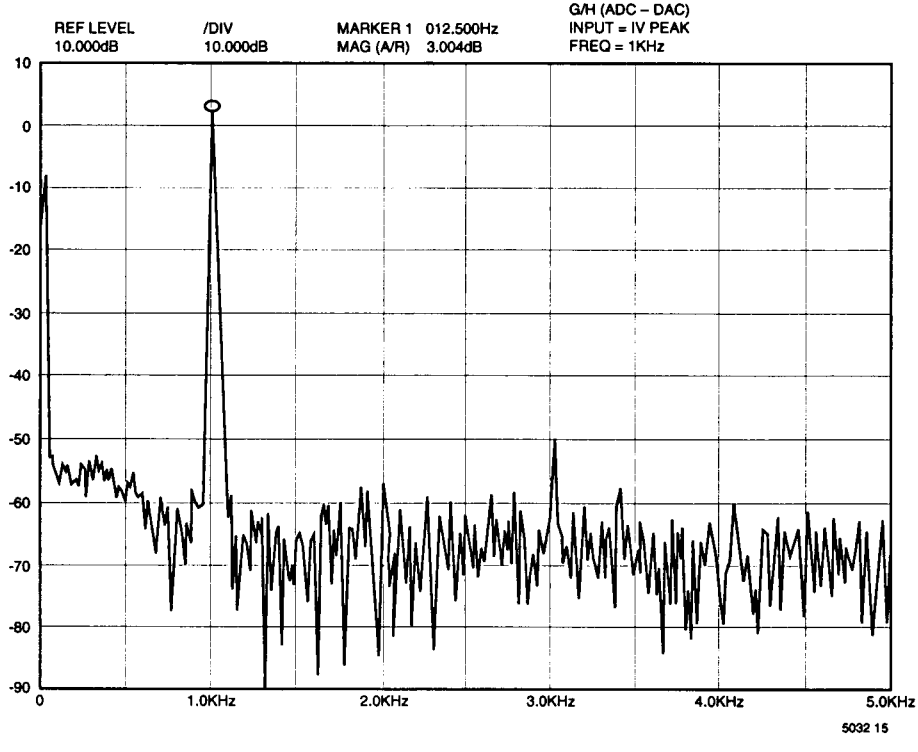


Figure 5. Output Signal Spectrum

NOTE: Applies when the 10-bit ADC and DAC are looped back and a 2Vpp 1KHz sinewave is applied to the receiver input: horizontal 500Hz/div, vertical 10dB/div.

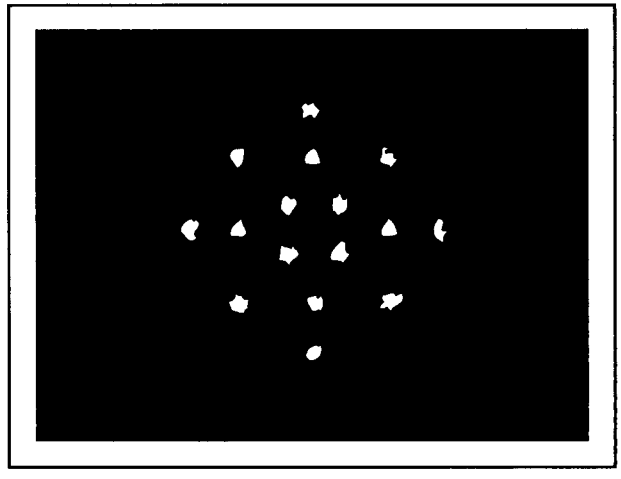


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Figure 6. 16-Point Signal Constellation for a 9600 bit/s Modem

SC11086/SC11196 INTERFACE REGISTERS

X	X	X	R2	R1	R0	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	
						D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	
			0	0	0	CABS2	CABS1	AGCFR	AGCTH	GEX	GI/$\overline{E}$	TL3	TL2	TL1	TL0	CONT1
			0	0	1	EYE/$\overline{TX}$	EYE R/$\overline{T}$	TDEN	EDLVL	TX1	TX0	AUZ	AUDIO	RX0	HYBON	CONT2
			0	1	0	TEST0	TEST1	TEST2	TDPLLJ	TDPLL INT/$\overline{EXT}$	TDPLL LOCK/$\overline{FREE}$	RDPLL SP1	RDPLL SP0	RDPLL1	RDPLL0	CONT3
			0	1	1	PA3	PA2	PA1	PA0	TFI2	TFI	M3	M2	M1	M0	CONT4
			1	0	0	EQT/$\overline{R}$	G8	G7	G6	G5	G4	G3	G2	G1	G0	PGC
			1	0	1	DX9	DX8	DX7	DX6	DX5	DX4	DX3	DX2	DX1	DX0	EYE X/TX
			1	1	0	DY9	DY8	DY7	DY6	DY5	DY4	DY3	DY2	DY1	DY0	EYE Y

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CONTROL REGISTERS

Register 000 – CONT1

FUNCTION	BIT #
CABS2	1 (LSB)
CABS1	2
AGCFR	3
AGCTH	4
GEX	5
GI/$\overline{E}$	6
TL3	7
TL2	8
TL1	9
TL0	10

CABS2, CABS1

Cable equalizer select one and two. These bits control a programmable cable equalizer according to Tables 1 and 2.

AGCFR

Freeze 1-bit AGC so that it will not react to amplitude changes.

AGCFR = 1 Freeze
AGCFR = 0 Active

AGCTH

1 bit AGC Threshold Control. Initially this bit should be zero. After the handshaking is complete the bit should be set to one.

AGCTH = 0 Narrow window (0.15–1.6V)
AGCTH = 1 Wide window (0.15–3.0V)

GEX

12dB Hybrid gain, externally controlled by the processor. (Effective only when GI/$\overline{E}$ = 0.)

GEX = 1 12dB
GEX = 0 0dB

CABS2	CABS1	LENGTH OF 0.4mm DIAMETER CABLE	
0	0	0	Bypass Cable Equalizer
0	1	1.8 km	Code 1
1	0	3.6 km	Code 2
1	1	7.2 km	Code 3

Table 1.

FREQUENCY (Hz)	CODE 1 (dB)	CODE 2 (dB)	CODE 3 (dB)
700	-0.99	-2.39	-3.93
1500	-0.2	-0.65	-1.22
2000	0.15	0.87	1.90
3000	1.43	3.06	4.58

Table 2. Gain Relative to 1700Hz/dB

GI/$\overline{E}$

12dB front end hybrid gain, controlled internally by the 1 bit AGC or externally by the processor.

GI/$\overline{E}$ = 1 Internal
GI/$\overline{E}$ = 0 External

TL3–TL0

Transmit level control.

TL3	TL2	TL1	TL0	LOSS (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	1	0	0	4
1	0	0	0	8

When TL0–TL3 = 0, the peak-to-peak transmit output level is ±3.2V.

Register 001 - CONT2

FUNCTION	BIT #
EYE/$\overline{TX}$	1 (LSB)
EYER/$\overline{T}$	2
TDEN	3
EDLVL	4
TX1	5
TX0	6
AUZ	7
AUDIO	8
RX0	9
HYBRON	10

EYE/$\overline{TX}$

Configures the transmit DAC to operate either in EYE pattern monitor or normal transmit mode.

EYE/$\overline{TX}$ = 1 EYE pattern mode
EYE/$\overline{TX}$ = 0 Transmit mode

EYER/$\overline{T}$

EYE pattern monitor strobe selector

EYER/$\overline{T}$ = 1 Receive strobe
EYER/$\overline{T}$ = 0 Transmit strobe

TDEN

Tone detector enable. Detects the presence of 1850Hz or 1650Hz tones while doing V.29 or V.27 demodulation.

TDEN = 1 Enabled
TDEN = 0 Disabled

EDLVL

Energy-detect level control.

EDLVL = 1 -43dBm on, -48dBm off
EDLVL = 0 -47dBm on, -52dBm off

TX1, TX0

Transmit path control.

TX1	TX0	PATH
0	0	Normal (modem transmit signal)
0	1	AUXTX
1	0	AUXTX + modem transmit signal
1	1	Squelch transmit

AUZ

Receive auto-zero; used to store the DC offset voltages of the I and Q channels.

AUDIO

Enable Audio Output.

RX0

Receive Section input control.

RX0 = 0 Normal
RX0 = 1 RXIN Grounded

HYBRON

Turn hybrid on. Used in G2 mode for simultaneous tone detection in the presence of transmit signal.

Register 010 - CONT3

FUNCTION	BIT #
TEST0	1
TEST1	2
TEST2	3
TDPLLJ	4
TDPLL INT/$\overline{EXT}$	5
TDPLL LOCK/$\overline{FREE}$	6
RDPLL SP1	7
RDPLL SP0	8
RDPLL1	9
RDPLL0	10

TEST0

TEST0 = 0 Normal mode is active
TEST0 = 1 Test mode is active and receive anti-aliasing filter output connects to transmit S/H stage. Also, adjusted sampling clock of RXDPLL will be brought out on RXCLK pin.

TEST1, TEST2

Test modes.

TEST1	TEST2	TEST MODE
0	0	Normal mode
0	1	Connect PGC output to AUDIO OUT
1	0	Connect I output to AUDIO OUT
1	1	Connect Q output to AUDIO OUT

TDPLLJ

Transmit PLL JAM. Reset the transmit DPLL on the next rising edge of the locking clock.

TDPLLJ = 1 JAM activated
TDPLLJ = 0 JAM deactivated

When the jam mode is activated by setting the TDPLLJ bit, the transmit phase locked loop will be reset on every positive transition of the input clock until TDPLLJ is reset by the controller.

TDPLL INT/$\overline{EXT}$, TDPLL Lock/$\overline{Free}$

Transmit phase locked loop control.

TDPLL INT/$\overline{EXT}$	TDPLL LOCK/$\overline{FREE}$	TEST MODE
X	0	Free run
1	1	TXSTROBE locked to receive strobe
0	1	TXSTROBE locked to external clock

RDPLLSP1, RDPLLSP0

Receive DPLL speed control.

RDPLL SP1	RDPLL SP0	SPEED
0	0	Fast (insert 8 clocks)
0	1	Slow1 (insert 1 clock per 1 baud)
1	0	Slow2 (insert 1 clock per 2 bauds)
1	1	Slow2 (insert 1 clock per 2 bauds)

RXDPLL Bandwidth

Mode / Baud Rate	SLOW[1]	NORMAL	FAST
2.4k	±0.0245% corr. = ±204 nsec	±0.049% corr. = ±204 nsec	±0.392% corr. = ±1634 nsec
1.6k[2]	±0.01634% corr. = ±204 nsec	±0.0327% corr. = ±204 nsec	±0.262% corr. = ±1634 nsec
1.2k	±0.0245% corr. = ±408 nsec	±0.049% corr. = ±408 nsec	±0.392% corr. = ±1634 nsec

NOTE 1: In slow mode, corrections will be integrated for two band periods. Therefore, the maximum effective correction (averaged per baud) will be half of the numbers given in the slow column of the table. This has been reflected in the bandwidth of the DPLL.

NOTE 2: Slow mode should not be used for the 1.6k baud rate, because the DPLL bandwidth goes below the ±0.02% required by the CCITT specification.

RDPLL0, RDPLL1

Receive DPLL Control.

RDPLL0	RDPLL1	TEST MODE
0	0	Free run
0	1	JAM
1	0	Hangup Detect Active
1	1	Normal

Register 011 - CONT4

FUNCTION	BIT #
PA3	1
PA2	2
PA1	3
PA0	4
TFI2	5
TFI	6
M3	7
M2	8
M1	9
M0	10

PA3–PA0

Receive DPLL phase adjustment control.

PA3 = 1 Advance
PA3 = 0 Retard

PA2	PA1	PA0	PHASE CHANGE
0	0	0	0°
0	0	1	9°
0	1	0	15°
0	1	1	24°
1	0	0	30°
1	0	1	39°
1	1	0	45°
1	1	1	54°

TFI2

This bit reduces the clock frequency of the RX low-pass and 2100Hz notch filters by a factor of 2. TFI2 is active only when the 2100Hz notch is inserted and TFI = 1.

TFI	TFI2	FUNCTION
0	X	Normal mode
1	0	Notch inserted, clock normal
1	1	Notch inserted, clock half of normal

TFI

Notch filter control. Inserts 2100Hz notch filter in the receive path. It is used in G2 mode for full duplex operation.

TFI = 1 Notch inserted
TFI = 0 Notch not inserted

M0–M3

Modem mode control (shown in Table 3).

MODE	DATA RATE	RXCLK	RXSTRB	TXCLK	TXSTRB	CARRIER	M3	M2	M1	M0
V.29	9600	9600	2400	9600	9600	1700	0	0	0	0
V.29FB1	7200	7200	2400	7200	9600	1700	0	0	0	1
V.29FB2	4800	4800	2400	4800	9600	1700	0	0	1	0
V.27	4800	4800	1600	4800	9600	1800	0	0	1	1
V.27FB	2400	2400	1200	2400	9600	1800	0	1	0	0
FSK, V.21	300	9600	9600	300	9600	1748.51	0	1	0	1
G2/G1	10368	10368	10368	10368	10368	—	0	1	1	0
Tone Gen	9600	9600	9600	9600	9600	—	0	1	1	1
V.33	14400	14400	2400	14400	9600	1800	1	0	0	0
V.33FB	12000	12000	2400	12000	9600	1800	1	0	0	1

Table 3.

Register 100

FUNCTION	BIT #
EQT/$\overline{R}$	1
G8	2
G7	3
G6	4
G5	5
G4	6
G3	7
G2	8
G1	9
G0	10

EQT/$\overline{R}$

Cable equalizer select between transmit and receive path.

EQT/$\overline{R}$ = 1 Equalizer in transmit path

EQT/$\overline{R}$ = 0 Equalizer in receive path

EYE DAC

The XDIS and YDIS are driven by the same DAC that generates the transmit S/H signal. Thus the X-Y display capability is enabled only when the transmitter is off. The update of the X-Y display can be controlled through the interface by the transmit or receive strobe. The EYE display needs to be updated only once per symbol period; in the case of the transmit strobe (9600Hz), the XDIS and YDIS are written once every (9600/symbol) sample. For the receive strobe which is equal to the symbol rate the X and Y displays are written once every strobe period. The sequence is illustrated in Figure 7.

G8	G7	G6	G5	G4	G3	G2	G1	G0	GAIN (dB)
1	0	0	0	0	0	0	0	0	24.08
0	1	0	0	0	0	0	0	0	12.04
0	0	1	0	0	0	0	0	0	6.02
0	0	0	1	0	0	0	0	0	3.01
0	0	0	0	1	0	0	0	0	1.50
0	0	0	0	0	1	0	0	0	0.75
0	0	0	0	0	0	1	0	0	0.37
0	0	0	0	0	0	0	1	0	0.18
0	0	0	0	0	0	0	0	1	0.09

An XDIS and YDIS written into the chip within a given strobe period will appear two strobes later. If neither X nor Y is written to the chip the X and Y displays will hold the previous values and will not be updated. If only one value (X or Y) is written into the chip both X and Y displays will be updated. The display which did not have its value changed will be updated according to the previous code in the corresponding register. When X or Y display is active the transmitter will be squelched. It will be activated on the rising edge of the first TX strobe that includes a transmit date; at that time X and Y displays will be squelched.

SERIAL INPUT

13 bits of control/data are shifted into the chip using 13 periods of SCLK. The data on SI pin must be valid on the falling edge of the SCLK. After SIEN goes low to high, the data on the SI pin is shifted into a 13-bit register on the falling edge of the SCLK. The timing is shown in Figure 8.

The MSB should be set first. After the 13th bit (LSB) is received, no further bits are shifted in until SIEN has another low-to-high transition.

The most significant 3 bits (Q13–Q11) are used for addressing as shown in Table 4.

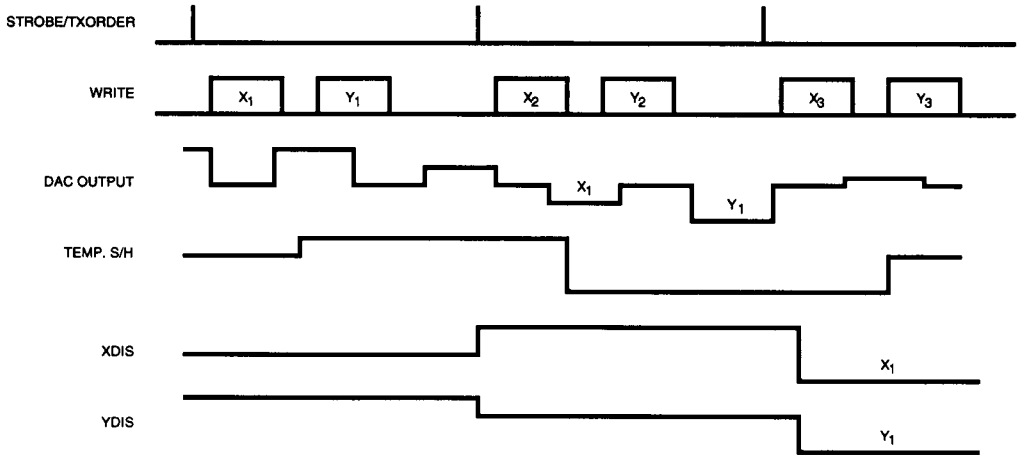
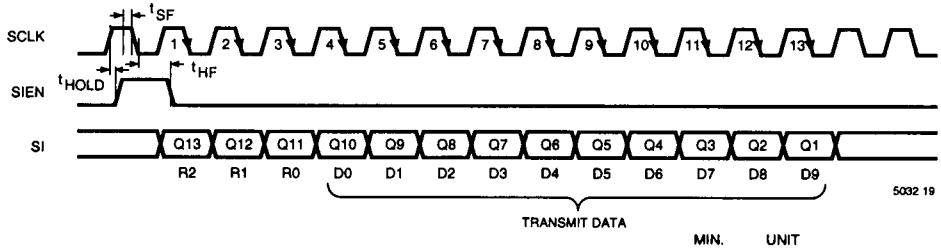


Figure 7. EYE DAC Sequence



		MIN.	UNIT
t_{HOLD}	HOLDING TIME FROM SERIAL CLOCK HIGH TO ENABLE HIGH	0	ns
t_{SF}	SETUP TIME FROM ENABLE HIGH TO SERIAL CLOCK LOW	50	ns
t_{HF}	HOLD TIME FROM SERIAL CLOCK LOW TO ENABLE LOW	100	ns
t_{SET}	SETUP TIME FROM STRB HIGH TO SIEN HIGH	0	ns

Figure 8. Serial Input Timing and Respect with STRB = TXSTROBE or RXSTROBE

NOTE: In TX = 1, SIEN can enable just after STROBE goes up. In TX = 0, SIEN can enable just after STROBE goes up by two times.

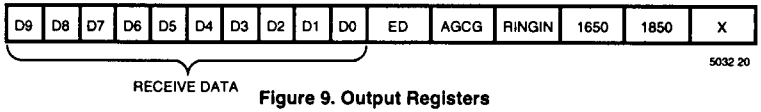


Figure 9. Output Registers

OUTPUT REGISTERS

Receive Data

D9–D0 are receive data from 10 bit ADC; D9 is MSB.

Q13–Q11	SOURCE AND DESTINATION
000	10 LSBs (Q10–Q1) loaded into CONTL1 register
001	10 LSBs (Q10–Q1) loaded into CONTL2 register
010	10 LSBs (Q10–Q1) loaded into CONTL3 register
011	10 LSBs (Q10–Q1) loaded into CONTL4 register
100	10 LSBs (Q10–Q1) loaded into PGC register
101	10 LSBs (Q10–Q1) loaded into EYEX/$\overline{TX}$ register
111	10 LSBs (Q10–Q1) loaded into EYEY register

Table 4.

ED

Energy detect output.

AGCQ

Gain of 1 bit AGC.

AGCG = 1 Gain is 12dB in receiver
AGCG = 0 Gain is 0dB in receiver

RINGIN

Ringin input.

1650

1650Hz tone detected.

1850

1850Hz tone detected.

SC11086/SC11196 INTERFACE TIMING I

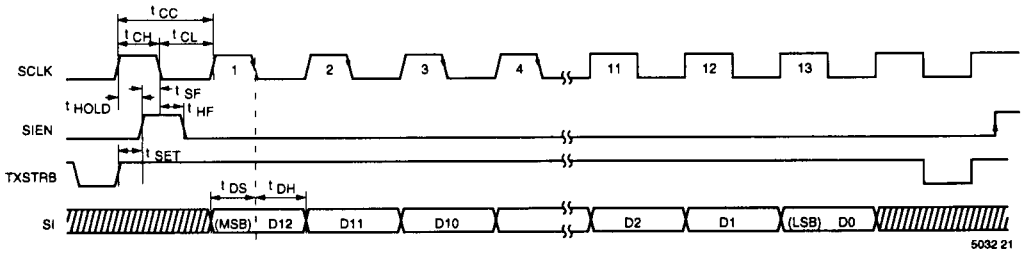


Figure 10. Serial Input Timing with Respect to TXSTRB

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CC}	Cycle Time of SCLK		408		ns
t_{CH}	SCLK High Period		204		ns
t_{CL}	SCLK Low Period		204		ns
t_{HOLD}	Holding Time From SCLK High to SIEN High	0			ns
t_{SF}	Set up Time From SIEN High to SCLK low	50			ns
t_{HF}	Holding Time From SCLK Low to SIEN low	100			ns
t_{SET}	Set up Time from TXSTRB High to SIEN High	0			ns
t_{DS}[1]	Data Setup Time with Respect to SCLK Low	104			ns
t_{DH}	Data Hold Time with Respect to SCLK Low			304	ns

NOTE 1: Only 13 bits of data are written serially into an internal shift register between two consecutive SIEN high pulses. It latches data which appear on the SI line using the falling edge of SCLK. The first three MSBs of D12, D11 and D10 represent a unique address of various internal data/control registers. The MSB is shifted in first.

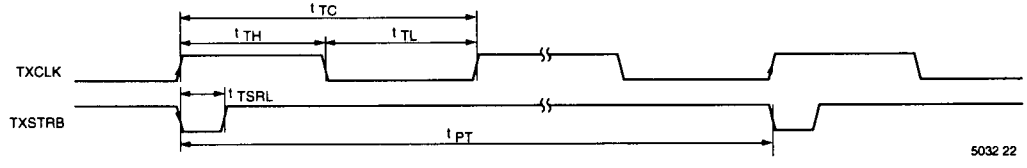


Figure 11. Transmit Clock Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{TC}[1]	Cycle Time of TXCLK	69.44		3,333	µsec
t_{TH}[2]	TXCLK High Period	34.72		1,667	µsec
t_{TL}	TXCLK Low Period	34.72		1,667	µsec
t_{TSRL}[3]	TXSTRB Low Pulse Width		17.36 or 12.05 or 10.4		µsec
$1/t_{PT}$[4]	Frequency of TXSTRB		9600 or 10368		Hz

NOTE 1: The frequency of TXCLK is varied from 300Hz to 14,400Hz according to operation modes (i.e. V.33, V.27FB or G2/G1, etc.).

NOTE 2: The TXCLK is a square wave with a typical duty cycle of 50%.

NOTE 3: 17.36ms of t_{TSRL} correspond to 9600Hz of $1/t_{PT}$ except for V.33 FB mode. It is 10.4ms of t_{TSRL} for V.33FB mode and 12.05ms of t_{TSRL} for G2/G1 mode.

NOTE 4: All TXSTRB frequencies are equal to 9600Hz except for G2/G1 mode which is 10368Hz.

SC11086/SC11196 INTERFACE TIMING II

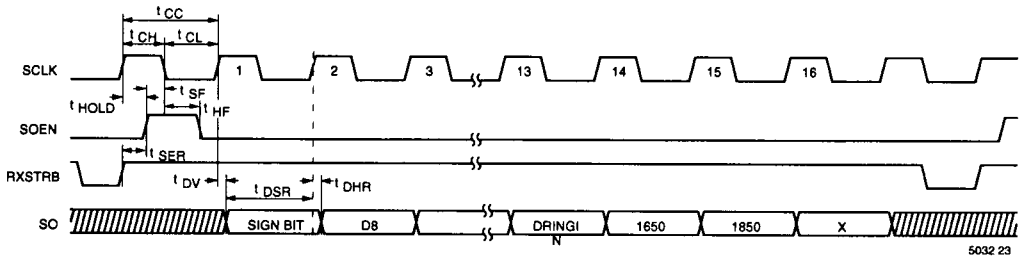


Figure 12. Serial Output Timing With Respect To RXSTRB

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CC}	Cycle Time of SCLK		408		ns
t_{CH}	SCLK High Period		204		ns
t_{CL}	SCLK Low Period		204		ns
t_{HOLD}	Holding Time from SCLK High to SOEN High	0			ns
t_{SF}	Set up Time from SOEN High to SCLK Low	50			ns
t_{HF}	Holding Time from SCLK Low to SOEN Low	100			ns
t_{SER}	Setup Time from RXSTRB High to Soen High	0			ns
t_{DV}	SO Data Valid after SCLK goes High			100	ns
t_{DSR}	Data Setup Time with Respect to SCLK High	304			ns
t_{DHR}[1]	Data Hold Time with Respect to SCLK High			100	ns

NOTE 1: A total of 16 bits of data are shifted out from an internal shift register between two consecutive SOEN high pulses. Data will be available after each rising edge of SCLK. The MSB is shifted out first. The LSB is don't care.

SC11086/SC11196 INTERFACE TIMING II (continued)

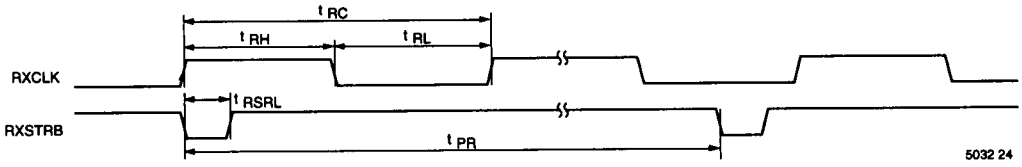


Figure 13. Receive Clock Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{RC}[1]	Cycle time of RXCLK	416.6		3,333	µsec
t_{RH}[2]	RXCLK High Period	208.3		1,667	µsec
t_{RL}	RXCLK Low Period	208.3		1,667	µsec
t_{RSRL}[3]	RXSTRB Low Pulse Width		6.9 or 13.8 or 12.05		µsec
$1/t_{PR}$[4]	Frequency of RXSTRB		2400 or 1600 or 1200 or 9600 or 10368		Hz

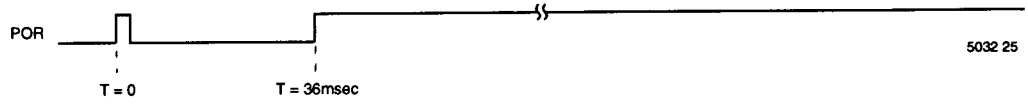
NOTE 1: The frequency of RXCLK is varied from 2400Hz to 14,400Hz according to operation modes (i.e. V.33, V.29, V.27 FB, etc.)

NOTE 2: The RXCLK is a square wave with a typical duty cycle of 50%.

NOTE 3: 6.9msec of t_{RSRL} correspond to all operation mode except for V.27FB mode, G2/G1 mode and FSK,V.21 mode. It is 13.8msec of t_{RSRL} for V.27FB mode. The RXSTRB will be the same as TXSTRB for the G2/G1 and FSK,V.21 modes. therefore, the t_{RSRL} will be identical to t_{TSRL} under the G2/G1 mode and FSK, V.21 mode. It is 12.05ms of t_{RSRL} for G2/G1 mode and 17.36ms of t_{RSRL} for FSK, V.21 mode.

NOTE 4: The frequency of RXSTRB is 2400Hz for V.33, V.33FB,V.29,V.29FB1I and V.29FB2 modes. The frequency of RXSTRB is 1600Hz for V.27 mode. The frequency of RXSTRB is 1200Hz for V.27FB and 9600Hz for FSK,V.21 mode. The frequency of RXSTRB is 10368Hz for the G2/G1 mode.

SC11086/SC11196 INTERFACE TIMING III



NOTE: Assume V_{DD} is turned on (V_{DD} > 3.75V) at T=0, POR pin goes low to activate the power-on-reset function for the DSP chip. After 36msec, the POR pin goes back to normally high until the V_{DD} drops below 3.5V.

Figure 14. Timing Diagram for Power-on-Reset pin (POR)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD} - V_{SS}$	12 V
DC Input Voltage (Analog Signals)	$V_{SS} - 0.6$ to $V_{DD} + 0.6$ V
DC Input Voltage (Digital Signals)	$V_{SS} - 0.6$ to $V_{DD} + 0.6$ V
Storage Temperature Range	–65 to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (Soldering 10 Sec.)	300°C

NOTE 1: Absolute maximum ratings are those values beyond which damage to the device may occur.
NOTE 2: Unless otherwise specified, all voltages are referenced to ground.
NOTE 3: Power dissipation temperature derating—Plastic package: –12 mW/C from 65°C to 85°C.

OPERATING CONDITIONS

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0	25	70	°C
V_{DD}	Positive Supply Voltage		4.5	5.0	5.5	V
A_{GND}, D_{GND}	Ground		-0.5	0	0.5	V
F_C	Clock Frequency		9.791	9.792	9.793	MHz
T_R, T_F	Input Rise or Fall Time	All digital inputs except CLK_{IN}		100	500	ns
T_R, T_F	Input Rise or Fall Time	CLK_{IN}		5	20	ns
V_{SS}	Negative Supply Voltage		-4.5	-5.0	-5.5	V

DC ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C, V_{DD} = +5V ± 10%, V_{SS} = -5V ± 10%)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Quiescent Current	Normal		19	36	mA
V_{IH}	High Level Input Voltage; Digital pins		2.4			V
V_{IL}	Low Level Input Voltage; Digital pins				0.8	V
V_{OH}	High Level Output (I_{OH} = 0.5 mA)		2.4			V
V_{OL}	Low Level Output (I_{OL} = 1.6 mA)				0.6	V
VXTA	Maximum Peak Output Level on TXA pin	V_{DD} = +5 V V_{SS} = -5 V	6	7.5	9	V_{PP}

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Mode	EDC = 0.47 µF; measured at RXA PGC = 0 dB				
Energy detect level (ED low to high)		-45	-44	-43	dBm
Loss of energy detect level (ED high to low)		-48	-47	-46	dBm
Hysterisis		2	3	5	dB

Programmable Gain Controller (PGC)

Gain step size		0.05	0.1	0.15	dB
Dynamic range		53	54	55	dB
Response time (from change in PGC register to output of A to D converter)			1.0	1.5	ms

Filter Characteristics

Crosstalk rejection		60	70	80	dB
Power supply rejection			40		dB
DPLL Response times JAM or FRZ Fast		10 150	20 200	30 250	µs µs
Low pass filter bandwidth		3.2	3.3	3.4	KHz